Code No. 3293

FACULTY OF ENGINEERING

B.E. 2/4 (CSE) First Semester (Suppl.) Examination, June/July 2011

LOGIC AND SWITCHING THEORY

Time : Three Hours] [Maximum Marks : 75

Note :— Answer **ALL** questions from Part A. Answer any **FIVE** questions from Part B.

PART—A (Marks : 25)

1. Convert the decimal number 369·3125 to Binary and Octal equivalent. 2
2. Implement F = AB' + A'B using NAND Gates. 3
3. Define Min term and Max term. 2
4. Perform the subtraction $(10)_{10} - (8)_{10}$ using 2's complement. 3
5. Distinguish between a Combinational logic circuit and Sequential logic circuit. 2
6. Explain the operation of 4-bit shift-register. 3
7. Write a VHDL Code for 2-to-4 Decoder. 3
8. Define Set-up time and Hold time. 2
9. Define and list the properties of a Symmetric function. 3
10. Define Symmetric network and draw the diagram for 3-variable function. 2

PART—B (Marks : 50)

11. Design the simplest :
    (a) Product-of-sums circuit that implements the function :
    $f(a, b, c) = \pi(0, 1, 5, 7)$. 5
    (b) Sum-of-products circuit for the function :
    $f(a, b, c) = \Sigma(3, 4, 6, 7)$. 5
12. (a) Derive the truth-table of an octal-to-binary priority encoder. 4
    (b) Implement the following Boolean function with 8-to-1 multiplexer and a single inverter :
    $F(A, B, C, D) = \Sigma(2, 3, 5, 6, 8, 9, 12, 14)$. 6

13. Using tabulation method, generate a set of prime implicants and find the minimal function for the following function :

$f(a, b, c, d) = \Sigma m(0, 2, 5, 7, 8, 10, 11, 14, 15)$. 10

14. Design a BCD to Excess-3 code converter using only NAND gates. 10

15. Design a sequential circuit that follows the state sequence 0, 1, 3, 6, 7, 5, 4, 2 using D flip-flops. 10

16. (a) Explain the operation of an Edge-triggered D flip-flop. 4

(b) Design a 4-bit Ripple Carry Adder. 6

17. Write short notes on the following :—

(a) Parity Generation and Checking 3

(b) Logic Simulation 3

(c) Binary Subtractor. 4