Code No. : 5342/S

FACULTY OF ENGINEERING
B.E. 2/4 (CSE) I Semester (Suppl.) Examination, July 2012
LOGIC AND SWITCHING THEORY

Time: 3 Hours] [Max. Marks : 75

Note : *Answer **all** questions from Part **A**, Answer **any five** questions from Part **B**.*

PART – A **(25 Marks)**

1. Simplity the following Boolean expressions to a minimum no. of literals. **2**

   a) $ABC + AB\overline{C} + \overline{A}B$.

   b) $\overline{(A+B).(\overline{A}+\overline{B})}$.

2. Represent the decimal numbers 694 and 835 in BCD and then show the steps necessary to form their sum. **3**

3. Draw the NAND logic diagram for the following expression
   $f = (\overline{A}B + C\overline{D}).E + B\overline{D}\,(A+B)$. **2**

4. Prove that the dual of the exclusive OR is also its complement. **3**

5. Differentiate between combinational and sequential circuits. **2**

6. Write a VHDL code for 4 to 1 multiplexer. **3**

7. Define the term clock skew. **2**

8. Draw the excitation table for SR flip-flop. **2**

9. Distinguish between a Synchronous counter and Ripple counter. **3**

10. What is the necessary and sufficient condition for a function to be symmetric ? **3**

PART – B (50 Marks)

11. Simplify the following function into sum-of-products and product-of-sums term.
$F(A, B, C, D) = \sum_m (2, 3, 5, 7, 8, 10, 12, 13)$. **10**

12. Derive the logic circuits for a 3-bit parity generator and 4-bit parity checker using an even parity bit. **10**

13. a) Distinguish between a Decoder and demultiplexer. **4**

    b) Design a 4-bit priority encoder circuit. **6**

14. By means of tabulation method, simplify the Boolean function. f(w, x, y, z) = $\sum_m (0, 2, 3, 5, 7, 8, 10, 11, 14, 15)$. **10**

15. Design an excess-3 code converter using NAND gates. **10**

16. a) Explain with a diagram about positive edge triggered D-type flip-flop. **5**

    b) Design a mod-8 counter with JK flip-flops. **5**

17. Write short notes on the following :

    a) Symmetric relay contact network. **5**

    b) 4-bit shift register. **5**
