Code No. : 6207

FACULTY OF ENGINEERING

B.E. II/IV (CSE) I SEMESTER (Main) Examination, Nov./Dec., 2009

LOGIC AND SWITCHING THEORY

Time : 3 Hours] **[Max. Marks : 75**

Note : Answer **all** questions from Part – A. Answer any **five** questions from Part – B.

PART – A (25 Marks)

1. Realize the following function using exclusive OR gates :

   $F = AB\bar{C}\bar{D} + A\bar{B}\bar{C}D + \bar{A}\bar{B}CD + \bar{A}BC\bar{D}$. 3

2. Convert the hexadecimal number 456 A to its decimal equivalent and the decimal number 9876 to its hexadecimal equivalent number. 2

3. Implement $F = \bar{x}y + x\bar{y} + z$ using NOR gates. 2

4. What are the advantages of tabulation method over Karnaugh map method of simplifying logic functions ? 3

5. Explain the concept of glitches when combinational circuits are used in conjunction with ripple counters with a suitable example. 3

6. Distinguish between a decoder and demultiplexer. 2

7. Draw the excitation table for a JK flip flop. Suggest a method of converting J K flip to D type flip flop. 3

8. Write a VHDL code for a 214 decoder. 3

9. Mention how a function can be symmetric with a suitable example. 2

10. Distinguish between a synchronous counter and ripple counter. 2

PART – B (50 Marks)

11. (a) Prove that the sum of all min terms of a 3 variable Boolean function is equal to 1.

    (b) Simplify the following expression :

    $F(A, B, C) = (A + B)\,\overline{(\bar{A} + \bar{B} + \bar{C})} + \bar{A}\bar{B} + \bar{A}\bar{C}$

    (c) Distinguish between sum of products and product of sums with an example. **3 + 4 + 3**

12. (a) Design a circuit using NAND gates only to realize
    $F(A, B, C, D) = ABC + BCD + ACD$

    (b) Repeat the above realization using only NOR gates. **5 + 5**

13. (a) Design a 5 × 32 decoder using only 3 × 8 decoder modules. Assume that each 3 × 8 decoder has one active low enable input and one active high enable input.

    (b) Distinguish between a decoder and encoder. **7 + 3**

14. Design a synchronous sequential circuit that follows the state sequence 0, 1, 3, 6, 7, 5, 4, 2. Realize the circuit using JK flip flops and NNAD gates. **10**

15. (a) Design a divide by 5 binary counter using JK flip flops. Plot the output waveform of each flip flop for a continuous input clock signal.

    (b) Develop a structural VHDL model for a 4 bit synchronous up/down counter. **6 + 4**

16. (a) Distinguish between prime implicants and essential prime implicants.

    (b) Simplify the logic function using Quine McClasky method : **3 + 7**

    $F(A, B, C, D) = \Sigma\, m(0, 1, 3, 7, 8, 9, 11, 15)$

17. Write short notes on the following : **10**

    (a) Ripple counter.

    (b) Symmetric relay contact network.

    (c) Asynchronous counter.
