Code No. : **3293**

FACULTY OF ENGINEERING

B.E. 2/4 (CSE) I Semester (Main) Examination, December 2010

LOGIC AND SWITCHING THEORY

Time : 3 Hours] [Max. Marks : 75

Note : *Answer* ***all*** *Questions from Part – A. Answer* ***any five*** *Questions from Part –* ***B.***

PART – A **(25 Marks)**

Answer **all** questions :

1. Specify the rules to be used to perform addition of two BCD numbers.
2. Convert the hexa decimal number 4ABC to its decimal number and the decimal number 9876 to its hexa decimal equivalent number.
3. Distinguish between a prime implicant and an essential prime implicant in the simplification of boolean expression using tabulation method.
4. Realize the following function using only XOR gates :

   $f = \overline{A}\ \overline{B}\ C\ D + \overline{A}\ B\ C\ \overline{D} + A\ \overline{B}\ \overline{C}\ D + A\ B\ \overline{C}\ \overline{D}$
5. Write a VHDL code for a 2 : 4 decoder.
6. Draw the circuit diagram of a full adder circuit using two half adders and the logic circuits.
7. Draw the truth (excitation) table of a JK flipflop.
8. Compare asynchronous and synchronous sequential logic circuits.
9. Draw the diagram of a 3 bit shift register and explain its operation.
10. What are the conditions to be satisfied for a function

    $f(x_1, x_2, x_3 \ldots\ldots x_n)$ to be symmetric ?

PART – B (50 Marks)

11. a) Distinguish between sum of products and product of sums with an example.

    b) Express the function $f(x,y,z) = y\bar{z} + xy + \bar{y}$ as a sum of product and product of sums.

    c) What do you understand by ASCII character set ? 3+4+3

12. a) What are the advantages of Quine Mc Clusky method over other methods of simplifying boolean expression ?

    b) Simplify $F(A, B, C, D, E) = \sum (2, 3, 7, 9, 11, 18, 23, 31)$ using K map technique. 3+7

13. a) Design a BCD to decimal decoder using NAND gates.

    b) Design a T flipflop, D flipflop and a JK flipflop using an SR flipflop. 5+5

14. a) Design a 5×32 decoder using only 3×8 decoder modules. Assume that each 3×8 decoder has one active low enable input and one active high enable input.

    b) Develop a structural VHDL model for a 4 bit synchronous up down counter. 5+5

15. a) Distinguish between a ripple counter and synchronous counter.

    b) Show that $f(x, y, z)=\sum (0, 3, 5, 6)$ is a symmetric function.

    c) Distinguish between a combinational circuit and sequential circuit. 3+4+3

16. Design a synchronous sequential counter that follows the state sequence 0, 1, 3, 6, 7, 5, 4, 2 using JK flipflop. 10

17. Write brief notes on 10

    a) Unite function

    b) Hazard free design

    c) Carry look ahead adder.