

Code No.: 6207

## FACULTY OF ENGINEERING B.E. 2/4 (CSE) I Semester (Suppl.) Examination, July 2010 LOGIC AND SWITCHING THEORY

| Tir   | me: 3 Hours]   | . [                     | Max. Marks:   | 75 |
|-------|--|-------------------------|---------------|----|
|       | Note: 1) Answer all questions from Part A. 2) Answer any five questions from Par                 | rt B.                   |               |    |
|       | PART - A   |                         |               | 25 |
| ***   | . Convert the decimal number 6789 to hexa decimal numb decimal number to its decimal equivalent. | er and conver           | t the hexa    | 2  |
| 2.    | . What do you understand by universal gates? Prove tuniversal gate.                              | that NAND g             | rate is a     | 3  |
| 3.    | Implement $F = \overline{xy} + x\overline{y} + z$ using NAND gates.                              |                         |               | 2  |
| 4.    | Define prime implicants and essential prime implicants.  |                         |               | 2  |
| 5.    | Design a full adder using full adders and other logic gate                                       | s.                      |               | 3  |
| 6.    | Distinguish between a combinational logic circuit and sec  | quential logic          | circuit.      | 3  |
| 7.    | Distinguish between a latch and flipflop.  |                         |               | 2  |
| 8.    | Compare the performance of sequential synchronous cir sequential circuits.                       | rali peliki a parabuk s | chronous      | 3  |
| 9.    | Give the block diagram of a 8 bit shift register with serial i                                   | n serial out an         | d parallel in | 3  |
| 10.   | State the conditions for a function to be symmetric.   |                         |               | 2  |
| (This | s paper contains 2 pages)  |                         | РТ (          | 7  |

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- 11. a) Given that  $R = P\overline{Q} + \overline{P}Q$ , prove that  $P = Q\overline{R} + \overline{Q}R$ .
  - b) Implement  $Q = R = P\overline{Q} + \overline{PQ} + S$  using NAND gates.
  - c) Explain with an example, the corrections used in BCD addition.

3+3+4

- 12. a) Give a circuit for the generation of odd parity of 8 bit character and explain its operation.
  - b) Simplify  $F(A,B,C,D,E) = \sum (2,3,7,9,11,18,23,31)$  using karmaugh map method. 3+7
- 13. a) Design a BCD to decimal decoder using only NAND gates.
  - b) Give the truth table of a full subtractor. Design a suitable circuit using only NOR gates.

5+5

- 14. a) Given a SR flipflop(s), design a JK flipflop, D flipflop and T flipflop using only SR flipflops.
  - b) Distinguish between synchronous and asychronous logic circuits.

8+2

15. a) Determine whether the following function is symmetric? Identify its number and variables of symmetry.

$$f(A,B,C) = \sum (0,2,3,4,5,7)$$

- b) What do you understand by a hazard in a contact network? Explain with an example.

  6+4
- 16. Using tabulation method, generate a set of prime implicants and find all minimal expressions for the following function.

$$f(P,Q,R,S,T) = \sum m(0,1,3,8,9,13,14,15,16,17,19,24,25,27,31)$$

10

10

- 17. Write short notes on the following:
  - a) Serial in parallel out shift register
  - b) ASCII character set
  - c) Binary multiplier (two bit)