Code No. 3294

FACULTY OF ENGINEERING

B.E. 2/4 (CSE) I-Semester (Supplementary) Examination, June/July 2011

COMPUTER ORGANIZATION ARCHITECTURE

Time : Three Hours] [Maximum Marks : 75

Answer **ALL** questions from Part-A.
Answer any **FIVE** questions from Part-B.

PART—A (Marks : 25)

1. Draw a block diagram for the add Micro-operation when implemented in a serial computer. Include two shift registers one full-adder and a flip-flop to store the carry. Assume that the carry flip-flop is initially cleared. 3
2. Show the representation of number –0·012 in IEEE floating point single-precision format. 2
3. Show different types of instruction formats and explain how they influence the system. 3
4. Mention the advantages of a Microprogrammed control unit organisation. 2
5. What are the effects of delay penalties in pipelining ? Illustrate with suitable examples. 3
6. Compare the characteristics of RISC with CISC. 3
7. Draw the circuit of a BCD adder. 2
8. Distinguish between Isolated and memory mapped I/O. 3
9. How does match logic function in Associative Memory ? 2
10. What is the function of TLB's in memory organisation ? 2

PART—B (Marks : 50)

11. Illustrate the design process of hardware implementation of accumulator. 10
12. A digital computer has a memory unit with a capacity of 8192 words, 36 bits per word. The instruction code format consists of 5-bits for the operation port and 13-bits for the address port (no indirect mode bit). Two instructions are packed in one memory word and a 36-bit instruction register IR is available in the control unit. Formulate the fetch and execute cycles for the computer. 10
13. (a) A 16-bit microprocessor has a single 16-bit bus which is shared for transferring either a 16-bit address or a 16-bit data word. Explain why an external address latch or register

would be required to store the address for memory unit. Formulate a possible set of control signals for communicating between microprocessor and memory. List the sequence of transfers for a memory read and a memory write cycles. 6

(b) Explain Booth's Multiplication algorithm. 4

14. (a) Describe in detail Interrupt methods of data transfer with multiple interrupt request. 5

(b) Explain the method of DMA transfer. How does a DMA controller improve the performance of a computer system ? 5

15. (a) Mention the importance of memory hierarchy using suitable examples.

(b) A computer system has a main memory of 1 M × 16 words and a 4K word Cache organised in the block-set-associative manner, with four blocks per set and 64 words per block.

(i) Calculate the number of bits in each of the TAG, SET and word fields of the main memory address format.

(ii) With Cache being initially empty, suppose that the CPU fetches 4352 words from locations 0, 1, 2 . . . . 4351, in that order. It then repeats this fetch sequence nine more times. If the Cache is 10 times faster than main memory, estimate the improvement factor resulting from the use of the Cache by using LRU block replacement algorithm. 5+5

16. (a) Explain the method of CPU-IOP communication in IBM 370. 4

(b) Interrupts and bus arbitration require to select one of several requests based on their priority. Design a circuit that implements a rotating priority. Scheme for flow input lines REQ1 to REQ4. Initially REQ1 has the highest and REQ4 the lowest priority. After some time if a line receives service, it becomes the lowest priority line and the next line receives the highest priority. Your circuit should generate four output grant signals GR1—GR4, one for each input request line. One of these outputs should be asserted when a pulse is received on a line called DECIDE. 6

17. Write short notes on :

(a) Micro-instruction formats

(b) Magnetic DISKS. 5+5