Code No. : 6208

FACULTY OF ENGINEERING

B.E. II/IV (CSE) I Semester (Main) Examination, Nov./Dec., 2009

COMPUTER ORGANIZATION AND ARCHITECTURE

Time : 3 Hours] **[Max. Marks : 75**

Note : Answer **all** questions from Part – A. Answer any **five** questions from Part – B.

PART – A (25 Marks)

1. Distinguish between half adder and full adder. 2

2. Show the hardware implementation of the following register transfer statements.

   T2 : A ← A + B

   T0 : A ← A + 1 3

3. What do you understand by micro instruction format ? 2

4. Show how a 9 bit micro operation field in a micro instruction can be divided into subfields to specify 48 micro operations. How many micro operations can be specified in a micro instruction ? 2

5. Explain the concept of memory interleaving and its advantages. 3

6. What is an instruction pipeline ? Explain with a suitable example. 3

7. Distinguish between isolated I/O and memory mapped I/O with an example. 2

8. What are the three methods of data transfer between an I/O peripheral device and memory ? Explain briefly with a suitable example. 3

9. How many PUSH and POP instructions are required to evaluate the expression P = (a * b) – (c/d + e) using reverse polish notation in a stack oriented computer. 3

10. What do you understand by match logic in an associative memory device. 2

PART – B (50 Marks)

11. (a) Explain the instruction cycle with an example.

    (b) Explain an interrupt cycle with an example. 5 + 5

12. (a) Distinguish between a general register organization and stack organization of a computer.

(b) Write an assembly language program to perform

$w = (P + Q/R) * (Q - S)$ using three/two/one/zero address instructions. **2 + 8**

13. (a) What is an array multiplier ?

(b) With the help of a block diagram, explain the process of addition/subtraction using two's complement number. **2 + 8**

14. With the help of a block diagram, explain in detail, the mechanism of data transfer between a peripheral device and memory in CPU. **10**

15. (a) Explain the direct mapping process of a cache memory of size 512×12 bits with a main memory of $32\ k \times 12$ bits. Give the relevant details.

(b) Draw the match logic for one word of associative memory and the corresponding logic diagram. **6 + 4**

16. (a) Explain indirect, indexed and based index addressing modes.

(b) Distinguish between CISC and RISC processors. **6 + 4**

17. Write brief notes on the following topics. **10**

(a) Interrupt

(b) Divide overflow

(c) Page replacement algorithm
