Code No. 2264

FACULTY OF ENGINEERING

B.E. 2/4 (CSE) I – Semester (Main) Examination, Nov./Dec. 2012

Subject: Computer Architecture

Time: 3 Hours **Max. Marks: 75**

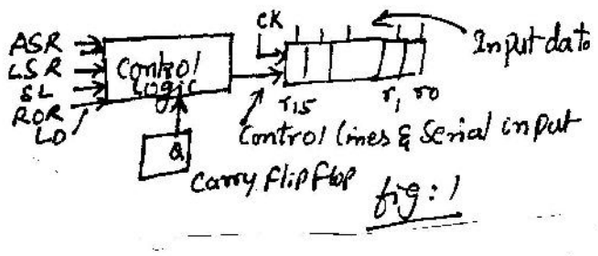
Note: Answer all questions from Part A. Answer any <u>five</u> questions from Part B.

PART – A (25 Marks)

1. Write reverse polish notation for the following:
   (A+B) ∗ [C∗ (D+E) + F] (2)
2. Draw a block diagram for the 'add' micro-operation when implemented in a serial computer. (2)
3. Explain arithmetic and divide overflow with some examples for 2'S complement numbers. (3)
4. Why is bus arbitration required? Write any two bus-arbitration methods. (3)
5. Write the IEEE 754 standard representation scheme for single and double precision floating point number. (3)
6. What are the various strategies for parallel processing in a computer? (2)
7. Explain Asynchronous communication interface. (2)
8. What is the difference between isolated I/0 and memory mapped I/0. Mention its advantages and disadvantages. (3)
9. A 128 MB main memory has a 64 KB direct-mapped cache with 16 bytes per line. How many liner are there in Cache and show main memory address bits are partitioned. (3)
10. What is Cache coherence? Mention the solutions to Cache coherence problem. (2)

PART – B (50 Marks)

11. Illustrate various paths available in the control unit with a flow chart. Summarize the paths that controls tasks during various computer cycles. (10)
12. An ALU of a processor uses shift register shown in the Fig. to perform shift and rotate operations. Inputs to the control logic for this register consist of: ASR: Arithmetic shift right, LSR: logic shift right, SL: shift left, RDR: rotate right, LD: parallel load. All shift and load operations are controlled by one clock input. The shift register is an edge triggered 'D' flip flop give the complete logic diagram for control logic for r_o, r_1 and r_{15}.



13. (a) Evaluate (A+B)∗(C+D) using 3, 2, 1, 0 address instruction. (6)
    (b) What is the use of fast multipliers? Write about array multipliers. (4)
14. (a) Explain the sequence of events that takes place after an interrupt occurs through flow chart. (6)
    (b) Differentiate between cycle stealing and burst mode transfer of DNA. (4)

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15.(a) Show how multiplication and division operations would be performed by hardware with a narrative flow chart. (6)

(b) Explain vector loops in a vector processor. (4)

16.(a) A two level memory system has 8-virtual pages on disk to be mapped into four page frames in the main memory. A computer programme generates the following page trace: 2,2,1,0,7,6,1,0,5,6,6,3,2,3,7,6 (i) sketch the successive pages residing in four page frames with respect to above page tracing using LRU replacement policy. Compute hit ratio also. (6)

(b) Show the hardware organization of associative memory and explain the read and write operation. (4)

17. Write short notes on:

a) Floating Point Arithmetic (5)

b) Array Processors. (5)

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