Code No. : 5343/N/S

FACULTY OF ENGINEERING
B.E. 2/4 (CSE) I Semester (New) (Suppl.) Examination, July 2012
COMPUTER ARCHITECTURE

Time : 3 Hours] [Max. Marks : 75

Note : *Answer **all** questions from Part **A**. Answer **any five** questions from Part **B**.*

PART – A **(25 Marks)**

1. The memory unit of a computer has 256 K words of 32 bit each. The computer has an instruction format with four fields 1 an operation code field, a mode field to specify one of seven addressing modes, a register address fields to specify one of 60 processor registers and a memory address. Specify the instruction format and the number of bits in each field if the instruction is in one memory word. **3**

2. Give the example of zero address, one address, two address and three address instructions. **3**

3. What are the types of control organizations ? **2**

4. What is meant by micro programmed control unit ? **2**

5. What is meant by pipelining and the advantage of pipelining ? **2**

6. Find the following 5-bit unsigned integer using non-restoring division : 10101/00101. **3**

7. What are the functions of a typical I/O interface ? **3**

8. Why does DMA have priority over the CPU when both request a memory transfer ? **3**

9. What is the function of a TLB ? **2**

10. How many 128×8 RAM chips are needed to provide a memory capacity of 2048 bytes ? **2**

PART – B (50 Marks)

11. Explain in detail the different types of instructions that are supported in a typical processor. 10

12. With neat diagram explain Von-Neumann computer architecture. 10

13. Explain in detail the working of a micro-programmed control unit. 10

14. Draw and explain the superscalar processors. 10

15. Explain in detail the principle of carry-look-ahead adder. Show how 16-bit CLA's can be constructed from 4-bit adders. 10

16. Explain the functions to be performed by a typical I/O interface with a typical input or output interface. 10

17. A digital computer has a memory unit of 64 K × 16 and a cache memory of 1 K words. The cache uses direct mapping with a block size of four words. How many bits are there in the tag, index, block and word fields of the address format ? How many blocks can the cache accommodate ? 10
