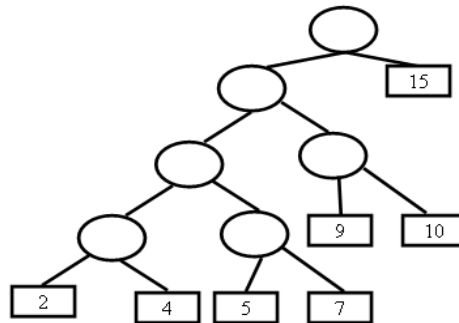


VARDHAMAN COLLEGE OF ENGINEERING**(AUTONOMOUS)**

Two Year M. Tech I Semester Supplementary Examinations September - 2012

(Regulations: VCE-R11)**DATA STRUCTURES AND ALGORITHMS****(Common to Computer Science and Engineering, Software Engineering)****Time: 3 hours****Max Marks: 60****Answer any FIVE Questions. All Questions carry equal marks****All parts of the questions must be answered in one place only**

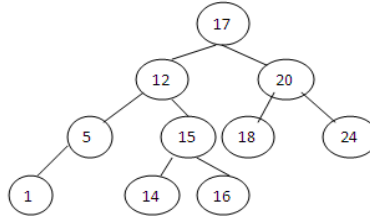
- 1 a) What is an equivalent infix form of the following postfix form of arithmetic expressions? 4M
 $ABC**DE+/F \uparrow$
 where \uparrow represents exponentiation
- b) If memory for the run time stack is only 150 cell (words), how big an 'n' be in n! before encountering a stack overflow? 4M
- c) What is a singly linked list? How do you represent a linked list? Write a 'C' program to create a singly linked list and display all the elements and find the number of elements in the list. 4M
- 2 Compute the efficiency of Merge Sort algorithm for best, average and worst cases. 12M
- 3 a) What is the nullity of a graph with n vertices? 4M
- b) Consider the following in-order and pre-order traversal of a binary tree. What is the post-order traversal of a binary tree? 4M
 In-order Traversal: D B F E G H A C
 Pre-order Traversal: A B D E F G H C
- c) Consider the following weighted binary tree: 4M



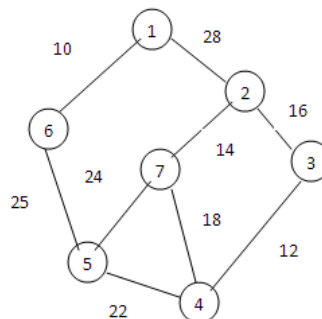
- i. What is the weighted external path length of the binary tree?
- ii. What is the weighted degree path length of the binary tree?

Cont...2

- 4 a) What is the average successful search time taken by binary search on a sorted array of 10 data items? 4M
- b) Consider an array: {25, 14, 16, 13, 10, 8, 12} represents a binary max-heap. What is the content of the array after two delete operations on a binary max-heap? 4M
- c) Consider the following balanced binary tree? 4M



- i. Mark the balance factor of each node on the above tree and state whether it is height balanced or not.
- ii. Insert an integer 13 into the above tree and show the new tree with the new balance factors on each node.
- 5 a) What is a splay tree? Explain, in detail, its operations and applications. 6M
- b) The Keys 12, 18, 13, 2, 3, 23, 5 and 15 are inserted into an initially empty hash table of length 10 using open addressing with hash function $h(k) = k \text{ mod } 10$ and linear probing. What is the resultant hash table? 6M
- 6 a) A natural merge sort is to be used to sort the file of integers: 12, 37, 42, 9, 5, 7, 50, 40, 45, 92. What is the order of the numbers after one pass of the sort? 4M
- b) The elements 32, 15, 20, 30, 12, 25 and 16 are inserted one by one in the given order into a Max Heap. What is the resultant Max Heap? 4M
- c) A complete, undirected, weighted graph G is given on the vertex set $\{0,1,2,\dots,n-1\}$ for any fixed 'n'. Draw the minimum spanning tree of G if:
- i. The weight of the edge (u, v) is $|u - v|$
- ii. The weight of the edge (u, v) is $u + v$
- 7 a) State the Kruskal's algorithm. 4M
- b) Find a minimum – cost spanning tree for every connected graph G using Kruskal's algorithm. 8M



- 8 a) Consider an undirected graph with vertex set $V=\{n_1, n_2, n_3, n_4, n_5, n_6, n_7, n_8\}$ and edge set $E=\{(n_1, n_2), (n_1, n_3), (n_1, n_4), (n_1, n_7), (n_2, n_3), (n_2, n_4), (n_2, n_5), (n_3, n_5), (n_3, n_6), (n_3, n_7), (n_4, n_5), (n_4, n_7), (n_5, n_6), (n_5, n_7), (n_5, n_8), (n_6, n_8), (n_7, n_8)\}$. Find the chromatic number of this undirected graph? 6M
- b) What is 8-queens problem? Give the solution for n-queens problem. 6M

VARDHAMAN COLLEGE OF ENGINEERING**(AUTONOMOUS)**

Two Year M. Tech I Semester Supplementary Examinations September - 2012

(Regulations: VCE-R11)**EMBEDDED SYSTEMS****(Common to Computer Science and Engineering, Software Engineering)****Time: 3 hours****Max Marks: 60****Answer any FIVE Questions. All Questions carry equal marks****All parts of the questions must be answered in one place only**

- 1 Embedded Systems are provided with plenty of peripherals and flash memory as well as RAM. Using these implement a working diagram for an automatic lift to handle four floors. Each floor has a key to record travel direction UP/DOWN. Inside the cabin a key board handles user requests and also a door closure/open key operations. Implement a generic design to optimize the lift operations. 12M
- 2 8051 processor has a Boolean processor with its own 128 bit accumulator. 12M
- a) Detail the bit level instructions and their use.
 - b) Using these instructions simulate
 - i. XOR GATE (Two input)
 - ii. NAND Gate (Two input)
- 3 a) Integrated Development Environments provide cross Assemblers, Linkers and simulators for easy program development. Explain the use of such tools to write and debug a programme. 6M
- b) Use BCD to Binary Conversion programme, to illustrate the use of directives and debug Tools. 6M
- 4 a) Large number of I/O lines is provided in 8051 to perform external I/O operations. Explain their programming. 6M
- b) Using I/O lines, and a driver circuit, write a programme to run a DC Motor or a Stepper Motor. Explain its operation. 6M
- 5 a) Interrupt are very important to service Time critical programmes. How do they operate use an example to illustrate 3M
- b) It is essential that a separate programme must oversee all tasks which need alteration on the basis of priority. Explain these with a practical example. 3M
- c) Explain the following states 3M
- i. Ready
 - ii. Eligible
 - iii. Deleted
 - iv. Blocked
- 6 Any real time programme uses multiple tasks working together in a main programme. Depending on time critical situations, A scheduler switches tasks without loss of context data. Explain how it is implemented in a real time programme. 12M

Cont...2

- 7 a) What are Assembler Directives? Give an example of their use in a programme development 3M
- b) What is a linker? How does it organize the object files of a numbering modules together? 3M
- c) The integrated development programme typically generates these following files 6M
- i. COF file (Common Objective Format)
 - ii. HEX file
 - iii. Map file
 - iv. A List file
 - v. Project file
- Explain their content and use.
How do you load your programme to flash memory?
- 8 a) ARM processor is in fact two processors in on chip ARM and THUMB. Explain why two processors are built in one system? 4M
- b) The ARM processor uses 32 bit code making it possible to provide multiple operations in a single instruction. Explain a few typical instructions. 4M
- c) The interrupt service is quite powerful in ARM. Explain the need for a fast interrupt service and a normal interrupt service with their own stack operations. 4M

VARDHAMAN COLLEGE OF ENGINEERING**(AUTONOMOUS)**

Two Year M. Tech I Semester Supplementary Examinations September - 2012

(Regulations: VCE-R11)**ADVANCED DATA COMMUNICATIONS****(Common to Digital Electronics and Communication Systems, Wireless and Mobile Communications)****Time: 3 hours****Max Marks: 60****Answer any FIVE Questions. All Questions carry equal marks****All parts of the questions must be answered in one place only**

- | | | |
|---|---|----|
| 1 | a) Determine
i. Peak frequency
ii. Minimum bandwidth
iii. Baud for a binary FSK Signal with a mark frequency of 49KHZ, a space frequency of 51KHZ and an i/p bit rate of 2kbps. | 6M |
| | b) For 16-PSK and a transmission system with a 10KHz bandwidth, determine the maximum bit rate. | 2M |
| | c) What is the purpose of a clock recovery circuit? When is it used? | 4M |
| 2 | a) Consider 8-QAM transmitter for modulation, give the bandwidth considerations, truth table phasor diagram and constellation diagram for the above mentioned modulation concept. | 8M |
| | b) The binary sequence 1100100010 is applied to the DPSK transmitter, Sketch the resulting waveform at the transmitter output. | 4M |
| 3 | a) Explain the four basic Network Topologies and advantage of each type. | 8M |
| | b) Explain about the Network Protocols and Standards. | 4M |
| 4 | a) Describe the Operation of UART transmitter. | 8M |
| | b) Explain the working of a start bit verification circuit. | 4M |
| 5 | a) Explain about statistical time division multiplexing. | 6M |
| | b) Briefly explain the following framing techniques
i. Added-digit framing
ii. Unique-line code framing | 6M |
| 6 | a) For a 12-bit data string of 101100010010 determine the number of Hamming bits requires, arbitrarily place the Hamming bits into the data string, determine the logic condition of each hamming bit, assume an arbitrary single-bit transmission error, and prove that the hamming code will successfully detect the error. | 7M |
| | b) Briefly describe the sliding window method of flow control. | 5M |
| 7 | a) Explain the BSC's polling sequences and selection sequences. | 6M |
| | b) Draw the structure of SDLC frame format. Explain in detail about SDLC control field. | 6M |
| 8 | a) Distinguish between Circuit Switching and Packet switching with necessary data formats. | 8M |
| | b) Draw a folded TDM bus having four lines. | 4M |

VARDHAMAN COLLEGE OF ENGINEERING
(AUTONOMOUS)

Two Year M. Tech I Semester Supplementary Examinations September - 2012
(Regulations: VCE-R11)

OPTICAL COMMUNICATION TECHNOLOGY
(Wireless and Mobile Communications)

Time: 3 hours

Max Marks: 60

Answer any FIVE Questions. All Questions carry equal marks
All parts of the questions must be answered in one place only

- | | | |
|---|--|----|
| 1 | a) Derive the wave equation for step index fiber and discuss the cut off conditions. | 6M |
| | b) Explain the microscopic and macroscopic bending losses in optical fibers and remedy steps. | 6M |
| 2 | a) What is meant by self phase modulation? Derive the expression. | 6M |
| | b) Explain the theory of four-wave mixing. | 6M |
| 3 | a) Explain the design of an isolator using faraday rotator. | 6M |
| | b) Explain the concept of Mach – Zehnder Inter ferometry and if a 2x2 MZI is used as a multiplexer for two WDM channels at a frequency separation of 10 GHZ, find the effective wave length difference. | 6M |
| 4 | a) Draw a setup for a typical Raman amplifier system and explain. | 6M |
| | b) Consider an In GaAsP semiconductor optical amplifier with width 5mM and thickness $0.5 \mu\text{m}$ and group velocity $2 \times 10^8 \text{ m/s}$. If a $1.0 \mu\text{w}$ optical signal at 1550 nm enters the device then find the photon density. | 6M |
| 5 | a) Explain the basic procedures for the cycle redundancy check (CRC) technique. | 6M |
| | b) Explain the fundamental concept of a coherent light wave system and also homodyne and heterodyne detection. | 6M |
| 6 | a) Calculate the maximum loss limited and dispersion limited distances of a link operating at 850 nm using the following components. <ul style="list-style-type: none"> i. Source: GaAiAs laser diode with Odbm fiber coupled power, $\Delta x = 2\text{nm}$, risetime = 1ns ii. Detector: Si APD with on sensitivity of -50dBm, risetime=2ns, capacitance of 1pf. iii. Fiber: Parabolic index multimode fiber with $\Delta = 0.01$, $n_1 = 1.46$ and loss of 3.5 db/km at 850 nm. iv. Two connectors with a loss of 1dB each. v. Splice every 2km with a loss of 0.1 dB / splice. Compare the systems operating at 100 Mbps and 200 Mbps. | 6M |
| | b) Write short notes on cross talk in an EDFA. | 6M |
| 7 | a) Discuss the concepts of stimulated Raman scattering and give the coupled equations. | 6M |
| | b) Write short notes on wavelength stabilization. | 6M |
| 8 | a) Explain how the zero dispersion wave length is shifted from $1.3 \mu\text{m}$ to $1.55 \mu\text{m}$. | 6M |
| | b) Write short notes on all optical networks. | 6M |

VARDHAMAN COLLEGE OF ENGINEERING
(AUTONOMOUS)

Two Year M. Tech I Semester Supplementary Examinations September - 2012
(Regulations: VCE-R11)

CPLD AND FPGA ARCHITECTURES AND APPLICATIONS
(Digital Electronics and Communication Systems)

Time: 3 hours

Max Marks: 60

Answer any FIVE Questions. All Questions carry equal marks
All parts of the questions must be answered in one place only

- | | | | |
|---|----|---|----|
| 1 | a) | Explain in brief about FPGA based system design? | 6M |
| | b) | Explain the basic logic programming elements of the FPGA with a suitable example? | 6M |
| 2 | a) | Why SRAM based FPGAs are popular when compared to other types? Explain? | 6M |
| | b) | Explain one time programmable (OTP) based FPGA? Explain its basic programming elements? | 6M |
| 3 | a) | Draw the Spartan-II I/O structure and explain its operation? | 6M |
| | b) | Explain the 2-input SRAM based LUT operation with the help of a suitable diagram? | 6M |
| 4 | a) | What are the key parameters to be considered while designing a logic circuit? | 6M |
| | b) | How these parameters are interrelated to each other and how to optimize the circuit for higher performance? | 6M |
| 5 | a) | Explain technology dependent optimization and its limitations? | 6M |
| | b) | How FPGA placement and routing is different from ASIC placement and routing process? | 6M |
| 6 | a) | Design 3-bit shift register, using FSM design? | 6M |
| | b) | Implement above design using Xilinx XC4000 FPGA? | 6M |
| 7 | a) | Explain PAL outputs with programmable polarity? | 6M |
| | b) | Explain the generic block diagram of complex PLD? | 6M |
| 8 | a) | Explain programmable routing matrix of Xilinx XC 4000 FPGA? | 6M |
| | b) | How sequential circuit is implemented in Altera Flex 8000 FPGA? | 6M |

VARDHAMAN COLLEGE OF ENGINEERING

(AUTONOMOUS)

Two Year M. Tech I Semester Supplementary Examinations September - 2012

(Regulations: VCE-R11)

POWER SEMICONDUCTOR DEVICES

(Power Electronics and Electric Drives)

Time: 3 hours

Max Marks: 60

Answer any FIVE Questions. All Questions carry equal marks
All parts of the questions must be answered in one place only

- 1 Discuss I-V characteristics and suitability of the following power switching devices. 12M
 i. BJT
 ii. MOSFET
 iii. IGBT
 iv. DIAC
- 2 a) Discuss about ratings and specifications of power diodes. 6M
 b) Two diodes are connected in series to share a total dc reverse voltage of $V_D=5KV$. The reverse leakage currents of two diodes are $I_{S1}=30mA$ and $I_{S2}=35mA$.
 i. Find the diode voltages if the voltage sharing resistances are $R_1=R_2=100k\Omega$.
 ii. Find the voltage sharing resistances R_1 & R_2 if the diode voltages are equal i.e
 $V_{D1}=V_{D2}=V_D/2$ 6M
- 3 a) Give the ON/OFF transition loss analysis of power transistor. 6M
 b) Explain in detail any two driver circuits used for power transistor. 6M
- 4 a) With neat circuits, explain the turn-on and turn-off characteristics of MOSFET. 6M
 b) Two MOSFETs are connected in parallel as shown in Figure 1, carry a total current of $I_T=30A$. The drain-to-source voltage of MOSFET M_1 is $V_{DS1}=4V$ and that of MOSFET M_2 is $V_{DS2}=4.5V$. Compute the drain current of each MOSFET and differences in current sharing if the current sharing series resistances are
 i. $R_{S1}=0.4\Omega$ and $R_{S2}=0.3\Omega$ and
 ii. $R_{S1}=R_{S2}=0.7\Omega$ 6M

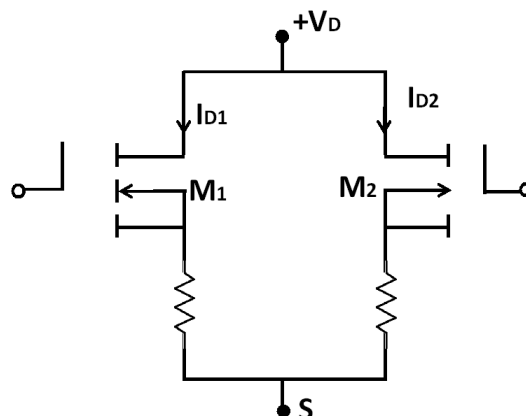


Figure. 1

- 5 a) Explain with the help of a neat diagram, the characteristics of insulated gate BJT. 6M
 b) Describe the structure and I-V characteristics of IGBT. 6M

Cont...2

- 6 a) Explain thyristor protection against 6M
i. Over voltages / currents
ii. di/dt
iii. dv/dt .
- b) Explain the switching characteristics and SPICE model of thyristor. 6M
- 7 a) Obtain electrical equivalent circuit of thermal model of a semiconductor device. 6M
b) A power device has a thermal capacity of $0.2J/^\circ C$ and a thermal resistance of $0.7^\circ C/W$. 6M
Determine the maximum power dissipation the power devices withstand for 0.1sec for a temperature not exceeding $40^\circ C$.
- 8 a) Briefly distinguish the design aspects of magnetic circuits from electrical circuits in semiconductor devices. 6M
b) Design the line frequency inductor for power semiconductor devices operation. 6M

VARDHAMAN COLLEGE OF ENGINEERING**(AUTONOMOUS)**

Two Year M. Tech I Semester Supplementary Examinations September - 2012

(Regulations: VCE-R11)**DISCRITE STRUCTURES AND AUTOMATA THEORY****(Computer Science and Engineering)****Time: 3 hours****Max Marks: 60****Answer any FIVE Questions. All Questions carry equal marks****All parts of the questions must be answered in one place only**

- 1 a) Prove or disprove the validity of the following argument using the rules of inference. 6M
 i. Every living thing is a plant or an animal
 ii. David's dog is alive and it is not a plant
 iii. All animals have hearts
 iv. Hence, David's dog has a heart
- b) With reference to automatic theorem proving, show that $S \vee R$ is tautologically implied 6M
 by $(P \cup Q) \cap (P \rightarrow R) \cap (Q \rightarrow S)$
- 2 a) If $A = \{1, 2, 3, 4\}$ and $B = \{a, b, c, d\}$, determine whether the following functions are 6M
 one-to-one or onto.
 1. $f = \{(1, a), (2, a), (3, b), (4, d)\}$
 2. $g = \{(1, d), (2, b), (3, a), (4, c)\}$
- b) Prove by pigeon hole principal that in a group of 61 people, at least 6 people were born 6M
 in the same month.
- 3 a) G is a group. Show that $f : G \rightarrow G$ is given by $f(x) = x^{-1}$, $\forall x \in G$ is an automorphism if 6M
 G is an abelian group.
- b) A man has 5 female and 7 male friends and his wife has 7 female and 5 male friends. In 3M
 how many ways can they invite 6 male and 6 female if husband and wife are to invite 6
 friends each.
- c) In how many ways can we distribute 10 red balls, 10 white balls and 10 blue balls in 6 3M
 different bowls.
- 4 a) Solve the recurrence relation $a_n - a_{n-1} + 10a_{n-2} = 0$ for $n \geq 2$, $a_0 = 1$ 6M
- b) Solve the r recurrence relation $a_n = a_{n-1} + n^3$ where $a_0 = 5$ by the method of substitution. 6M
- 5 a) Prove or explain with the help of an algorithm that "every NFA will have an equivalent 6M
 DFA".
- b) Minimize the FA given below and show that given and reduced are equivalent. 6M

Note: Assume that q_0 as start state
 and q_6 as final state.

State	a	b
q_0	q_0	q_3
q_1	q_2	q_5
q_2	q_3	q_4
q_3	q_0	q_5
q_4	q_0	q_6
q_5	q_1	q_4
q_6	q_1	q_3

:: 2 ::

- 6 a) Give a regular expression for the set of all strings over $\{a, b\}$ accepting all strings which have number of a's divisible by 6 and number of b's divisible by 8. 6M
- b) What do you mean by ambiguity? Show that the grammar $S \rightarrow S/S, S \rightarrow a$ is ambiguous. 6M
- 7 a) Convert the following in GNF $S \rightarrow AB, A \rightarrow BS/b, B \rightarrow SA/a$ 8M
- b) Construct PDA that accepts the language $L = \{0^n 1^m / n \neq m, n, m \geq 1\}$ 4M
- 8 a) Design a Turing Machine that accepts the set of all even palindromes over $\{0, 1\}$. 6M
- b) What is decidability? Explain any two undecidable problems. 6M

VARDHAMAN COLLEGE OF ENGINEERING
(AUTONOMOUS)

Two Year M. Tech I Semester Supplementary Examinations September - 2012
(Regulations: VCE-R11)

ENERGY CONVERSION SYSTEM
(Power Electronics and Electric Drives)

Time: 3 hours

Max Marks: 60

Answer any FIVE Questions. All Questions carry equal marks
All parts of the questions must be answered in one place only

- | | | |
|---|--|----------|
| 1 | a) Discuss the features of PV system and their applications
b) At 300 K in silicon, the intrinsic carrier concentration in $n_i = 1.45 \times 10^{16}/m^3$. The impurity charge concentration are $N_d = N_a = 10^5 n_i$. Estimate barrier voltage, barrier width and maximum field across the barrier. [$k = 1.38066 \times 10^{-23}$ J/K = 8.617×10^{-5} eV/K, $q = 1.6022 \times 10^{-19}$ coul, $\epsilon_0 = 8.842 \times 10^{-12}$ F/m, $\epsilon_r = 12$ for Si] | 6M
6M |
| 2 | a) Write short notes on open and closed loop cycle MHD system.
b) Calculate the open CKT voltage and maximum power output of MHD generator of plate area 0.2 m^2 . The gas is moving with uniform velocity 1000 m/s between the plate at 0.5 m apart in the magnetic field 2 wb/m^2 . Assume the conductivity of the gas is $10^3/\text{m}$ | 5M
7M |
| 3 | a) Describe with a neat sketch the working of a wind energy system (WECS) with main components.
b) Discuss the wind characteristics, performance and limitations of energy conversion systems. | 6M
6M |
| 4 | a) Discuss working of a turbine employed for tidal power generation.
b) Discuss the existing tidal projects briefly. | 6M
6M |
| 5 | a) Explain the various wave energy systems with examples.
b) Describe the closed cycle OTEC system, with its advantages over open cycle system. | 6M
6M |
| 6 | a) Discuss the environmental impact of geo-thermal energy?
b) How seebeck coefficients vary with temperature. | 6M
6M |
| 7 | a) Derive an expression for EMF of fuel cell
b) Describe how the following energy storage schemes work. <ul style="list-style-type: none"> i. Pumped Hydro scheme ii. Compressed air | 6M
6M |
| 8 | a) What are the different classes of Batteries. Explain the principle of working of a battery.
b) Describe a lead-acid battery. Explain the advantages of batteries bulk energy storage. | 6M
6M |

VARDHAMAN COLLEGE OF ENGINEERING**(AUTONOMOUS)**

Two Year M.Tech I Semester Supplementary Examinations September - 2012

(Regulations: VCE-R11)**DISCRITE STRUCTURES AND AUTOMATA THEORY****(Software Engineering)****Time: 3 hours****Max Marks: 60**

Answer any FIVE Questions. All Questions carry equal marks
All parts of the questions must be answered in one place only

- 1 a) Prove or disprove the validity of the following argument using the rules of inference. 6M
 i. Every living thing is a plant or an animal
 ii. David's dog is alive and it is not a plant
 iii. All animals have hearts
 iv. Hence, David's dog has a heart
- b) With reference to automatic theorem proving, show that $S \vee R$ is tautologically implied by $(P \cup Q) \cap (P \rightarrow R) \cap (Q \rightarrow S)$ 6M
- 2 a) Show that for any two sets A and B $p(A) \cup p(B) \subseteq p(A \cup B)$ 6M
 b) Let $f(x) = x + 2$, $g(x) = x - 2$ and $h(x) = 3x$ for $x \in \mathbb{R}$, where \mathbb{R} is the set of real numbers. Find $g \circ f$; $f \circ g$; $f \circ f$; $h \circ g$; $f \circ h \circ g$ 6M
- 3 a) Show that the intersection of any two congruence relations on a set is also a congruence relation. 6M
 b) How many terms are there in the formula for two number of elements in the union of 10 set given by the principle of inclusion and exclusion. 6M
- 4 a) Solve the recurrence relation. $S(k) - 10.S(k-1) + 9.S(k-2) = 0, S(0) = 3, S(1) = 11$. 8M
 b) Find coefficient of x^9 in $(1+x^3+x^8)^{10}$. 4M
- 5 a) Explain the differences between NFA and DFA. 6M
 b) Design a DFA which accepts all strings which are ending with 101 over an Alphabet $\{0,1\}$. 6M
- 6 a) Construct a FA recognizing the following regular grammar. 6M
 $S \rightarrow aS / bA / b$
 $A \rightarrow aA / bS / a$
 b) List the closer properties of regular sets and explain any two of them 6M
- 7 a) Define Deterministic pushdown automata and design a PDA that accepts the language $a^n b^n (n \geq 1)$ 3M
 b) Define CNF and convert the following CFG into CNF 9M
 $S \rightarrow Abc / Bc$ $A \rightarrow aa$ $B \rightarrow bb$
- 8 a) Design a Turing machine which multiplies two integers. Give its state transition diagram also. 8M
 b) Write short notes on LBA. 4M

VARDHAMAN COLLEGE OF ENGINEERING**(AUTONOMOUS)**

Two Year M. Tech I Semester Supplementary Examinations September - 2012

(Regulations: VCE-R11)**OBJECT ORIENTED ANALYSIS AND DESIGN****(Software Engineering)****Time: 3 hours****Max Marks: 60****Answer any FIVE Questions. All Questions carry equal marks****All parts of the questions must be answered in one place only**

- | | | |
|---|--|-----|
| 1 | a) Write and explain the principles for modeling. | 6M |
| | b) Explain the four common mechanisms that will be applied for the UML. | 6M |
| 2 | a) Explain how to model the class diagram with an example. | 6M |
| | b) Explain the common mechanisms that are used in basic structural modeling. | 6M |
| 3 | What are interaction diagram? What are contents and common properties present in interaction diagrams? | 12M |
| 4 | a) Explain the different terms used in use case modeling. | 6M |
| | b) Discuss in detail about the forking and joining. | 6M |
| 5 | Enumerate the steps to model the following | |
| | a) Modeling an API | 6M |
| | b) Modeling tables, files and documents. | 6M |
| 6 | What is iterative incremental development? Why is it requiring in software development process? Explain. | 12M |
| 7 | a) Explain the inception phase in unified software development? | 6M |
| | b) Explain about archetypal elaboration of iteration workflow. | 6M |
| 8 | Draw and explain the following diagram for library information system | |
| | a) Class diagram | 6M |
| | b) Sequential diagram | 6M |

VARDHAMAN COLLEGE OF ENGINEERING**(AUTONOMOUS)**

Two Year M. Tech I Semester Supplementary Examinations September - 2012

(Regulations: VCE-R11)**ADVANCED DIGITAL SIGNAL PROCESSING****(Common to Digital Electronics and Communication Systems and Wireless and Mobile Communications)****Time: 3 hours****Max Marks: 60****Answer any FIVE Questions. All Questions carry equal marks****All parts of the questions must be answered in one place only**

- | | | |
|---|--|-----|
| 1 | a) What are the differences between FIR and IIR filters | 6M |
| | b) Find the parallel form realization of the following | 6M |
| | $H(z) = \frac{3z(5z-2)}{(z+\frac{1}{2})(3z-1)}$ | |
| 2 | a) Explain about decimation and interpolation with necessary derivations. | 6M |
| | b) What are the applications of multi rate signal processing? | 6M |
| 3 | a) Explain about Levinson Durbin Algorithm. | 6M |
| | b) What are the properties of Linear prediction filters? | 6M |
| 4 | Consider ARMA process generated by the difference equation
$X(n)=1.6x(n-1)-0.6x(n-2)+w(n)+0.9w(n-1)$ | |
| | a) Determine the system function of the whitening filter and its poles and zeros. | 6M |
| | b) Determine the power spectral density of x(n). | 6M |
| 5 | a) Explain in detail LMS algorithm for direct FIR filters. | 6M |
| | b) Explain the Adaptive equalization concept. | 6M |
| 6 | Explain power spectrum estimation by ARMA model? | 12M |
| 7 | What is the difference between causal and non-causal IIR Wiener filters. Explain about wiener convolution. | 12M |
| 8 | Write the Statement of Kalman filtering problem and derive the related expressions? | 12M |

VARDHAMAN COLLEGE OF ENGINEERING**(AUTONOMOUS)**

Two Year M. Tech I Semester Supplementary Examinations September - 2012

(Regulations: VCE-R11)**PRINCIPLES OF MACHINE MODELING ANALYSIS****(Power Electronics and Electric Drives)****Time: 3 hours****Max Marks: 60****Answer any FIVE Questions. All Questions carry equal marks****All parts of the questions must be answered in one place only**

- | | | | |
|---|----|--|----|
| 1 | a) | Explain the Per Unit representation of generalized machines. | 6M |
| | b) | Explain Basic two axis representation of synchronous machines. | 6M |
| 2 | a) | What is primitive machine? Illustrate briefly the primitive form of various machines. | 6M |
| | b) | Derive the torque equation in basic two pole machine. | 6M |
| 3 | a) | Derive the transient analysis of a separately excited D.C. motor | 6M |
| | b) | Obtain an electrical circuit which is equivalent to a separately excited D.C Motor. | 6M |
| 4 | a) | Explain the active transformation ($\alpha, \beta, 0, d, q, 0$) | 6M |
| | b) | Obtain the derivation for transformed impedance matrix. | 6M |
| 5 | a) | Explain a mathematical model of a 3-phase induction motor and write the voltage equations. | 6M |
| | b) | Derive a torque equation of a 3- ϕ induction motor in a state space form | 6M |
| 6 | a) | Derive the voltage and torque equation in machine variables. | 6M |
| | b) | Explain the steady-state analysis of the operation of a three phase induction motor. | 6M |
| 7 | a) | Describe induction motor dynamics during starting and braking. | 6M |
| | b) | Derive the equation for the dynamical response of the induction motor. | 6M |
| 8 | a) | Determine the performance characteristic of the machine in an actual axis to transformation form. | 6M |
| | b) | A 3-Phase star connected 50Hz, synchronous generator has direct-axis synchronous reactance of 0.65PU and quadrature axis synchronous reactance of 0.5pu. The generator delivers rated KVA at rated voltage. Calculate open circuit voltage and voltage regulation at 0.8P.F. Resistance drop at full load is 0.02pu. | 6M |

VARDHAMAN COLLEGE OF ENGINEERING**(AUTONOMOUS)**

Two Year M. Tech I Semester Supplementary Examinations August - 2012

(Regulations: VCE-R11)**COMPUTER ARCHITECTURE AND ORGANIZATION****(Computer Science and Engineering)****Time: 3 hours****Max Marks: 60****Answer any FIVE Questions. All Questions carry equal marks****All parts of the questions must be answered in one place only**

- | | | | |
|---|----|--|----|
| 1 | a) | Draw the block diagram of a 4-bit Bidirectional shift register with parallel load. Write the function table and explain its operation. | 6M |
| | b) | Simplify the function $F(A,B,C)=\sum(0,2,6)$ with don't cares $d(A,B,C)=\sum(1,3,5)$ | 6M |
| 2 | a) | What are the error detection codes? Convert the decimal 225.225 to octal and hexadecimal. | 6M |
| | b) | What is a multiplexer? With a logic diagram explain working of 4 by 1 multiplexer. | 6M |
| 3 | a) | What are the register transfer logic languages? Explain few RTL statements for branching with their actual functioning. | 5M |
| | b) | Define addressing modes. Explain all the addressing modes with an example. | 7M |
| 4 | a) | Write the HDL description of Booth's multiplexer algorithm for 8 bit operands. | 6M |
| | b) | Draw the data path of a floating point arithmetic unit. Write the algorithm for floating point addition. | 6M |
| 5 | a) | With a neat block diagram, explain the operations of AMD2909 bits-sliced microprocessor sequencer. | 6M |
| | b) | Draw and explain 2-level control store organization for nano programming. | 6M |
| 6 | a) | What is virtual memory technique? Explain the different virtual memory techniques. | 4M |
| | b) | Explain how the technique of paging can be implemented. | 8M |
| 7 | a) | Draw the block diagram of a DMA controller and explain the functioning. | 6M |
| | b) | Describe the serial communication protocol RS232. | 6M |
| 8 | a) | Draw and explain the hypercube interconnection network for multiprocessors. | 6M |
| | b) | Describe the architecture of a shared memory multiprocessor. | 6M |

VARDHAMAN COLLEGE OF ENGINEERING**(AUTONOMOUS)**

Two Year M. Tech I Semester Supplementary Examinations September - 2012

(Regulations: VCE-R11)**SOFTWARE REQUIREMENTS AND ESTIMATION****(Software Engineering)****Time: 3 hours****Max Marks: 60****Answer any FIVE Questions. All Questions carry equal marks****All parts of the questions must be answered in one place only**

- | | | |
|---|--|----------|
| 1 | Good practices adopted for software requirements engineering represent highly effective ways for software professionals". Justify. Also explain the elements of software risk management. | 12M |
| 2 | a) What is meant by requirements elicitation? Discuss the elicitation techniques.
b) Discuss about setting requirements priorities. | 6M
6M |
| 3 | What is requirement Traceability Matrix? What are the steps to be considered to implement requirement traceability on a project? | 12M |
| 4 | a) Explain the requirements management principles and procedures.
b) Represent the links between requirements and other system elements in requirements Traceability Matrix. What are the specific steps to be considered to implement requirements traceability on a specific project? | 6M
6M |
| 5 | a) List out the benefits in using requirements Management Tools?
b) Draw the figure how the requirements Management Tools integrate with other kinds of software tools. Explain about Rational Requisite Pro. | 6M
6M |
| 6 | What is meant by estimation? Discuss the necessity for software estimation. What are the problems associated with estimation? Discuss them in detail. | 12M |
| 7 | a) Discuss clearly the Full Function Point method of software estimation
b) Discuss the following concepts in respect of software estimation | 6M
6M |
| 8 | a) What are the various estimation factors and approaches to effort and schedule estimation? Write about Putnam estimation Model.
b) Explain the desirable features in software estimation tools. Write about COCOMO II. | 6M
6M |

VARDHAMAN COLLEGE OF ENGINEERING**(AUTONOMOUS)**

Two Year M.Tech I Semester Supplementary Examinations September - 2012

(Regulations: VCE-R11)**SOFTWARE ENGINEERING****(Computer Science and Engineering)****Time: 3 hours****Max Marks: 60**

**Answer any FIVE Questions. All Questions carry equal marks
All parts of the questions must be answered in one place only**

- | | | |
|----|--|-----|
| 1 | a) What are the fundamental software process activities? | 4M |
| | b) Explain the SEI approach of a company's software engineering practices. | 6M |
| | c) Discuss on the statement: "The only deliverable for a successful project is the working program". | 2M |
| 2. | Explain about various evolutionary process models and specify examples. | 12M |
| 3 | a) Explain Basic and Intermediate COCOMO model of Software estimation. | 6M |
| | b) Explain Class – Responsibility – Collaborator Modeling. | 6M |
| 4 | Explain the design steps in transform mapping and transaction mapping with examples. | 12M |
| 5 | Describe the interface design guidelines for | 12M |
| | i. General interaction | |
| | ii. Information display | |
| | iii. Data input. | |
| 6 | a) Explain unit testing and Integration testing. | 6M |
| | b) Describe software verification and validation. | 6M |
| 8 | a) What are software configuration items? | 4M |
| | b) What is software quality? What are SQA activities? | 4M |
| | c) What are software risks? How will you identify them? | 4M |

VARDHAMAN COLLEGE OF ENGINEERING**(AUTONOMOUS)**

Two Year M. Tech I Semester Supplementary Examinations September - 2012

(Regulations: VCE-R11)**SOFTWARE PROCESS AND PROJECT MANAGEMENT****(Software Engineering)****Time: 3 hours****Max Marks: 60****Answer any FIVE Questions. All Questions carry equal marks****All parts of the questions must be answered in one place only**

- | | | | |
|---|----|---|----|
| 1 | a) | What is the need for optimizing the software process? How this optimization process will be balanced in the software maturity frame work? | 6M |
| | b) | Compare the Defined process and Optimized process levels in software maturity frame work. | 6M |
| 2 | a) | Justify "Software process change rests on many of the principles of organizational change". | 6M |
| | b) | Illustrate the principles of software process change and explain each briefly. | 6M |
| 3 | a) | Explain the process of optimizing the software cost parameters to increase the software 'ROI'. | 8M |
| | b) | What are the long standing debates among developers and vendors of software cost estimation tools. Explain in detail. | 4M |
| 4 | a) | State and explain various artifacts of the project management process. | 9M |
| | b) | Write short notes on Test Artifacts. | 3M |
| 5 | a) | Explain the Iteration emphasis on the software life cycle. How the iteration process planning will be done for various phases. | 5M |
| | b) | How the concurrency among the stake holders will be achieved using major mile stones of the software process? | 7M |
| 6 | a) | Explain about the fundamental flaws that are suffered by conventional work breakdown structures. Describe the solution in detail. | 6M |
| | b) | What is meant by "line of business organizations"? Write the roles and responsibilities of these organization people. | 6M |
| 7 | a) | Explain the Management and Engineering perspectives to assess whether the project is "on budget and on schedule". | 8M |
| | b) | Write about the basic characteristics of good pragmatic software metrics. | 4M |
| 8 | a) | List and explain the critical approaches of modern process framework for resolving Top Ten risks. | 6M |
| | b) | Define "Culture Shifts". How the cultural shifts must be overcome to transition from conventional SPM process to a modern SPM process. | 6M |

VARDHAMAN COLLEGE OF ENGINEERING**(AUTONOMOUS)**

Two Year M. Tech I Semester Supplementary Examinations September - 2012

(Regulations: VCE-R11)**ARTIFICIAL INTELLIGENCE AND NEURAL NETWORKS****(Common to Computer Science and Engineering, Software Engineering)****Time: 3 hours****Max Marks: 60****Answer any FIVE Questions. All Questions carry equal marks****All parts of the questions must be answered in one place only**

- | | | |
|---|---|-----|
| 1 | a) What is Best First Searching? Explain the detail A* Algorithm. | 6M |
| | b) What are Blind Search Procedures and Heuristic Search strategies? Explain with Examples. | 6M |
| 2 | Trace the constraints satisfaction procedure solving the following crypt arithmetic problem:
CROSS
+ ROADS

DANGER | 12M |
| 3 | a) Explain the four ways of parsing the following sentence. "Have the students who missed the exam take it today". | 6M |
| | b) Describe ATN parsing procedure with example. | 6M |
| 4 | Explain in detail the process involved in knowledge acquisition to build an expert system. | 12M |
| 5 | a) Explain signal flow graph model of Neural Network. | 6M |
| | b) Explain the procedure of knowledge representation in a Neural Network. | 6M |
| 6 | a) What is a supervised and un supervised learning? Explain learning with teacher. | 6M |
| | b) Explain probably approximately correct model of learning. | 6M |
| 7 | a) What is perceptron model of neural network? Explain why XOR problem can't be solve by perceptron model of neural network. | 6M |
| | b) Explain the Idealized Learning Curve of the LMS Algorithm. | 6M |
| 8 | a) Explain the accelerated convergence of Back Propagation Learning algorithm. | 4M |
| | b) Briefly explain complexity Regularization Technique for Network Pruning. | 8M |

VARDHAMAN COLLEGE OF ENGINEERING**(AUTONOMOUS)**

Two Year M.Tech I Semester Supplementary Examinations September - 2012

(Regulations: VCE-R11)**EMBEDDED SYSTEMS****(Computer Science and Engineering, Software Engineering)****Time: 3 hours****Max Marks: 60**

Answer any FIVE Questions. All Questions carry equal marks
All parts of the questions must be answered in one place only

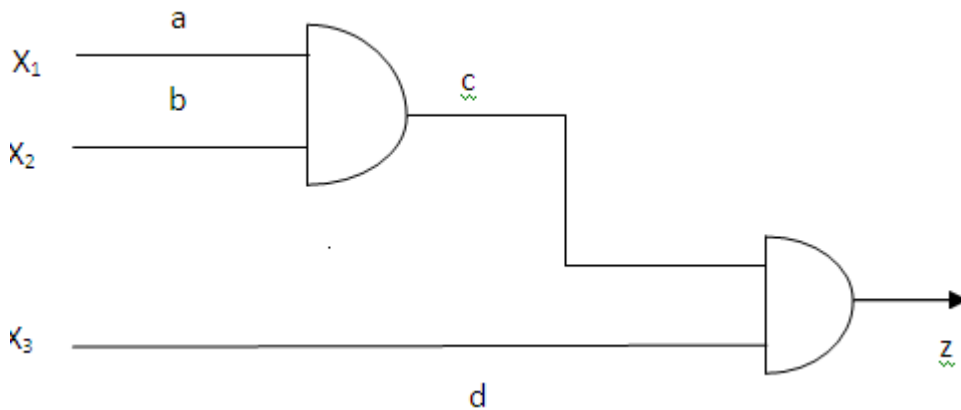
- | | | |
|---|--|----------------|
| 1 | An automatic coin operated weighing machine starts the measurement sequence on dropping a coin. It measures the displacement of the plat form to estimate the load. Using the peripherals in any embedded processor such as Timers, Counters, ADC, design a block diagram to perform the weighing and output a printed card. | 12M |
| 2 | a) Explain the organising 8051 micro controller.
b) i. Give two conditions under which program OP codes are fetched from external, rather than internal memory.
ii. Give the bit addressing, bit 4 of RAM byte 2Ah. | 6M
6M |
| 3 | a) i. Move the data in addresses 10h to addresses 20h to 2Ah. For example move the data at address 10h to address 20h and so on until data address 11Ah is moved to 2Ah.
ii. Treat registers R0 and R1 as 16bit register(R0=LSB, R1=MSB) and rotate them one place to left; i.e. bit 7 of R0 becomes bit 0 of R1, bit 7 of R1 becomes bit 0 of R0.
b) i. Explain the various jump statements.
ii. Add the byte in external RAM location 02CDh to internal RAM location 19h; put the result into external RAM locations, 00C0h (MSB) treat the source data and results are in BCD. | 6M
6M |
| 4 | a) Explain the use of I/O ports in 8051, for outputting a data or reading a data.
b) Using a PORT, implement a 4 X 4 key matrix key board with key encoding and decoding. | 6M
6M |
| 5 | a) Interrupt are very important to service Time critical programmes. How do they operate use an example to illustrate
b) It is essential that a separate programme must oversee all tasks which need alteration on the basis of priority. Explain these with a practical example.
c) Explain the following states
i. Ready
ii. Eligible
iii. Deleted
iv. Blocked | 3M
3M
3M |
| 6 | Any real time programme uses multiple tasks working together in a main programme. Depending on time critical situations, A scheduler switches tasks without loss of context data. Explain how it is implemented in a real time programme. | 12M |
| 7 | a) What are Assembler Directives? Give an example of their use in a programme development
b) What is a linker? How does it organize the object files of a numbering modules together?
c) The integrated development programme typically generates these following files
vi. COF file (Common Objective Format)
vii. HEX file
viii. Map file
ix. A List file
x. Project file
Explain their content and use.
How do you load your programme to flash memory? | 3M
3M
6M |
| 8 | a) Briefly explain SHARC processor programming model w.r.t registers, instruction of groups, addressing modes.
b) Explain I ² C bus. | 6M
6M |

VARDHAMAN COLLEGE OF ENGINEERING**(AUTONOMOUS)**

Two Year M. Tech I Semester Supplementary Examinations September - 2012

(Regulations: VCE-R11)**DIGITAL SYSTEMS DESIGN****(Digital Electronics and Communication Systems)****Time: 3 hours****Max Marks: 60****Answer any FIVE Questions. All Questions carry equal marks****All parts of the questions must be answered in one place only**

- | | | |
|---|--|----|
| 1 | a) Compare the Karnaugh-map and programmed minimization methods. | 6M |
| | b) How timing and static hazards are minimized? | 6M |
| 2 | a) Using PLA implement half adder circuit. | 6M |
| | b) Implement a full-adder circuit with a decoder and two OR gates. | 6M |
| 3 | a) Implement the following function with a multiplexer:
$F(A, B, C, D) = \sum(0, 1, 3, 4, 8, 9, 15)$. | 6M |
| | b) Show that a full adder can be constructed with two half-adders and an OR gate. | 6M |
| 4 | a) State the differences between D-latch and positive-edge-triggered D-Flip-Flop | 6M |
| | b) Explain clocked synchronous state machine design process. | 6M |
| 5 | a) Explain race condition in sequential circuit design? How to overcome this issue? | 6M |
| | b) State the timing issues in sequential circuit design? | 6M |
| 6 | a) Discuss in detail about State Machine (SM) charts with example. | 6M |
| | b) Construct an SM block that has three input variables (D, E, F), four output variables (P, Q, R, S), and two exit paths. For this block, output P is always 1, and Q is 1 if D=1 and F are 1 or if D and E are 0, R = 1 and exit path 2 is taken. If (D=0 and E=1) or (D=1 and F=0), S=1 and exit path 1 is taken. | 6M |
| 7 | a) Draw the table giving the set of all possible single stuck faults and the faulty and fault-free responses and also construct the fault cover table for the circuit shown in below. | 6M |



- | | | |
|---|---|----|
| | b) Discuss in detail about bridging fault model with examples. | 6M |
| 8 | a) Explain the procedure involved in D-algorithm with an example. | 6M |
| | b) With an example explain about the transition count testing method. | 6M |

VARDHAMAN COLLEGE OF ENGINEERING**(AUTONOMOUS)**

Two Year M. Tech I Semester Supplementary Examinations September - 2012

(Regulations: VCE-R11)**TELECOMMUNICATION SWITCHING SYSTEMS AND NETWORKS****(Wireless and Mobile Communications)****Time: 3 hours****Max Marks: 60****Answer any FIVE Questions. All Questions carry equal marks****All parts of the questions must be answered in one place only**

- | | | |
|---|--|----|
| 1 | a) With the aid of necessary figures and derivations explain the functionality of simple telephone communication system. | 6M |
| | b) Explain basics of switching systems | 6M |
| 2 | a) Differentiate single stage and multistage network. | 6M |
| | b) Determine the design parameters of a three stage switch with inlet utilization of 0.1 to achieve a $P_B=0.0002$ for (i) $N=128$ (ii) $N= 2048$ | 6M |
| 3 | a) Explain how combination switching is better than time multiplexed space switching and time multiplexed time switching and also derive the expression for probability of blocking for combination switching. | 6M |
| | b) Calculate maximum access time that can be permitted for data and control memories in TSI switch with single input and output trunk multiplexing 2500 channels and also estimate cost of the switch and compare it with that of single stage. | 6M |
| 4 | a) Explain the methods commonly used for deciding on the route for a particular connection and compare them. | 6M |
| | b) Explain the different types of signaling techniques involved in a telecommunication networks. | 6M |
| 5 | a) Explain CCITT no.7 signaling system with a block schematic diagram and compare with OSI seven layer model | 6M |
| | b) Explain principle and operating of out band signaling and in band signaling in FDM carrier system and compare them. | 6M |
| 6 | a) Explain about different types of ring networks. | 6M |
| | b) An Ethernet operates at 10Mbits/s. It is 1 km length and velocity of propagation is 2×10^8 m/s. Data packets consist of 512 bits, including a 64 bit overhead. A receiving terminal takes the time of one bit access the channel in order to send acknowledgement signal, which consists of an empty packet. If there are no collisions at what rate the system convey data? | 6M |
| 7 | a) Explain traffic mathematical model of telephone communication system. | 6M |
| | b) On an average one call carries every 5s. During a period of 10s what is the probability that <ul style="list-style-type: none"> i. No call arrives ii. One call arrives iii. Two calls arrives iv. More than two calls arrives | 6M |
| 8 | a) Explain about network and protocol architecture of ISDN. | 6M |
| | b) Explain about significance of functional groups and reference points of ISDN | 6M |

VARDHAMAN COLLEGE OF ENGINEERING**(AUTONOMOUS)**

Two Year M. Tech I Semester Supplementary Examinations September - 2012

(Regulations: VCE-R11)**CMOS VLSI DESIGN****(Digital Electronics and Communication Systems)****Time: 3 hours****Max Marks: 60****Answer any FIVE Questions. All Questions carry equal marks****All parts of the questions must be answered in one place only**

- | | | |
|---|---|-----|
| 1 | a) Explain the current-voltage characteristics of MOSFET based on Square law model. | 6M |
| | b) Calculate the native threshold voltage for an n-transistor at 300 ⁰ k for a process with a Si substrate with $NA=1.80 \times 10^{16}$, a SiO ₂ gate oxide with thickness 200 Å. Assume $\Phi_{ms}=-0.9v$, $\Phi_{fc}=0$, $Ni=1.45 \times 10^{10} \text{ cm}^{-3}$. | 6M |
| 2 | a) Derive the propagation delay times of a CMOS inverter for low to high and high to low transitions. | 6M |
| | b) Consider a CMOS inverter with the following parameters: V _{dd} =5V, NMOS: $V_{TO,n}=0.6V$, $\mu_n C_{ox}=60\mu A/V^2$, (W/L) _n =8 PMOS: $V_{TO,p}=-0.7V$, $\mu_p C_{ox}=25\mu A/V^2$, (W/L) _p =12. Calculate the critical voltages (V _{OL} , V _{OH} , V _{IL} , V _{IH}) on the VTC and find the noise margins of the circle | 6M |
| 3 | a) Explain the complementary pass transistor logic and draw the schematic of 2 input NAND gate using CPL. | 6M |
| | b) Write the difference between pass transistor logic and Transmission gate logic. Realize the given Boolean function using CMOS Transmission gate logic.
$F=AB+A'C'+AB'C$ | 6M |
| 4 | a) Design and explain the operation of 2 input CMOS NAND gate. | 6M |
| | b) Design a CMOS 1-bit Full adder Circuit. | 6M |
| 5 | a) Draw and explain the operation of CMOS Pseudo static D flip-flop. | 6M |
| | b) Draw a transmission gate based storage circuit using EFET's and explain its operation. | 6M |
| 6 | a) Prove that "A C ² - MOS register with CLK-CLK' clocking is insensitive to overlap". | 6M |
| | b) Discuss the charge-sharing problems in VLSI circuits. Explain various circuit techniques used in domino CMOS circuits for solving charge-sharing problems. | 6M |
| 7 | Write short notes on | 12M |
| | i. Charge sharing and charge leakage problems | |
| | ii. Pre charge / evaluate logic | |
| | iii. Domino logic gate characteristics | |
| 8 | a) Draw the circuit of 2 input AND/NAND gate using basic CVSL logic and explain it. | 6M |
| | b) What are the advantages and disadvantages in using Dual-Rail logic networks? | 6M |

VARDHAMAN COLLEGE OF ENGINEERING**(AUTONOMOUS)**

Two Year M. Tech I Semester Supplementary Examinations September - 2012

(Regulations: VCE-R11)**INTERNETWORKING AND INTERNET PROTOCOLS****(Wireless and Mobile Communications)****Time: 3 hours****Max Marks: 60**

Answer any FIVE Questions. All Questions carry equal marks
All parts of the questions must be answered in one place only

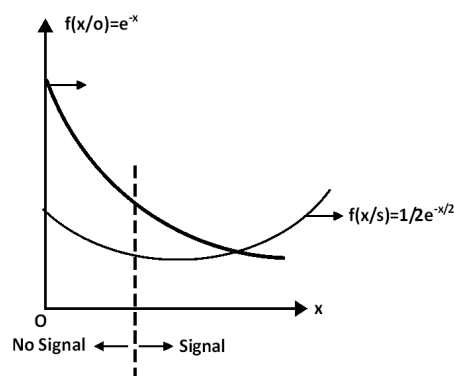
- | | | | |
|---|----|---|----|
| 1 | a) | What are the OSI Reference Model layers? Illustrate how the higher layers will be serviced by the lower layers. | 8M |
| | b) | Compare and Contrast the OSI reference model and TCP/IP reference model. | 4M |
| | a) | What is a subnet? Explain in detail about need for subnet in a network. | 4M |
| 2 | b) | Elaborate the classful and classless addressing. | 4M |
| | c) | Explain the ARP protocol in detail. | 4M |
| 3 | a) | Compare and contrast IPv4 and IPv6 protocols briefly. | 6M |
| | b) | Differentiate transparent and non transparent fragmentation techniques. | 6M |
| 4 | a) | State and explain Stream Control Transmission Protocol. | 4M |
| | b) | Explain Multicast Open Shortest Path Forward (MOSPF) Protocol with an example | 8M |
| 5 | a) | What is multicasting? List various applications of Multicasting. | 6M |
| | b) | State and explain the Multicast Routing with an Example. | 6M |
| 6 | a) | Discuss the Network Virtual Terminal Mechanism to solve the access to remote Computer. | 8M |
| | b) | Explain the Name Address Resolution in the Internet. | 4M |
| 7 | a) | Explain SMTP Architecture and its services in detail. | 6M |
| | b) | Differentiate direct and indirect Mobile IP | 6M |
| 8 | a) | Illustrate different compression techniques for Audio and Video without using original clarity. | 6M |
| | b) | What is the need of Proxy server in a network? How it improves network performance? | 6M |

VARDHAMAN COLLEGE OF ENGINEERING**(AUTONOMOUS)**

Two Year M. Tech I Semester Supplementary Examinations September - 2012

(Regulations: VCE-R11)**DETECTION AND ESTIMATION THEORY****(Common to Digital Electronics and Communication Systems, Wireless and Mobile Communications)****Time: 3 hours****Max Marks: 60****Answer any FIVE Questions. All Questions carry equal marks****All parts of the questions must be answered in one place only**

- | | | | |
|---|----|--|----|
| 1 | a) | List out any four properties of receiver operating characteristics for simple binary hypothesis tests | 6M |
| | b) | Explain bays criterion for M hypothesis. | 6M |
| 2 | a) | Explain the effect of sampling the band limited random signal. | 6M |
| | b) | Define and explain periodic random processes with necessary equations. | 6M |
| 3 | a) | Explain for the simple binary case the optimum receiver can be realized as a matched filter or a correlation receiver with neat diagrams. | 6M |
| | b) | For general binary case the optimum receiver can be realized as a matched filter or a pair of filters? | 6M |
| 4 | a) | Derive the solution for the optimum receiver for the simple binary detection problem of a known signal in non white Gaussian noise. | 6M |
| | b) | Explain joint MAP estimates in additive white Gaussian noise channel. | 6M |
| 5 | a) | A single observation $x=s+n$ consists of zero mean Gaussian noise plus either $s^{(1)}=1$ (or) $s^{(2)}=2$, with the two possible signals equally likely to be present
Show that the best minimum P_e decision rule says that $s^{(1)}$ is present if $x \leq 1.5$ and $s^{(2)}$ is present if $x > 1.5$
Find the corresponding P_e if $\sigma_n^2 = 1$ | 6M |
| | b) | One sample of x is taken. If $x > d$, signal is declared present as shown in figure | 6M |



- Show that if $d=2$, the false alarm probability is 0.135 (probability that noise alone is mistaken for signal)
- Find the probability of detection (probability that signal, when present is correctly detected) for $d=2$.

:: 2 ::

- 6 a) Explain multi dimensional problem with any one of the example. 6M
b) Explain colored noise estimation? 6M
- 7 Discuss with suitable derivation , the estimation of signal parameter using recursive linear mean squared estimation. Assume that the signal is random in nature. 12M
- 8 Let $r(u) = \sqrt{p}a(u) + n(u)$ for $-\infty < u < t$, where $a(u)$ & $n(u)$ are uncorrelated zero mean stationary processes and 12M
- $$s_a(\omega) = \frac{2k}{\omega^2 + k^2} \text{ and } s_n(\omega) = \frac{N_0}{2}.$$
- The desired signal is $d(t) = a(t+\infty)$. Find
- i. The optimum(MMSE) realizable filter
 - ii. The normalized prediction error

VARDHAMAN COLLEGE OF ENGINEERING**(AUTONOMOUS)**

Two Year M. Tech I Semester Supplementary Examinations September - 2012

(Regulations: VCE-R11)**POWER ELECTRONIC CONVERTERS-1****(Power Electronics and Electric Drives)****Time: 3 hours****Max Marks: 60****Answer any FIVE Questions. All Questions carry equal marks****All parts of the questions must be answered in one place only**

- | | | |
|---|--|-----|
| 1 | a) Describe how the concept of a thyristorised AC voltage Controller can be utilized as a on load tap Changing transformer. | 6M |
| | b) A single phase AC voltage controller with R-L load has the following details:
Supply voltage = 230V, 50HZ, $R=4\ \Omega$ and $\omega L=3\Omega$. Calculate
(i) the control range of firing angle.
(ii) the maximum value of RMS load current, and (iii) the maximum power and power factor. | 6M |
| 2 | Explain the operation of the three phase AC full wave voltage controller with waveforms and develop the governing equations when $\alpha=60^\circ$ and 120° | 12M |
| 3 | a) Describe three-phase to three –phase cycloconverter with relevant circuit arrangements using 18 thyristors and 36 thyristors. What are the advantages of three phase bridge cycloconverter circuit over three-phase to three-phase cycloconverter circuit consisting of 18 SCRs. | 6M |
| | b) List out merits and demerits of cycloconverter. | 6M |
| 4 | a) With neat circuit diagram and wave forms explain the Single-Phase dual converter | 6M |
| | b) Distinguish between dual converter with and without circulating current mode of operation using proper circuit diagrams. | |
| 5 | a) Derive an expression for output voltage of a single phase fully controlled bridge converter by conducting the following factors:
(i) Overlap angle (ii) Source inductance. | 6M |
| | b) Explain the operation of three phase twelve pulse converter along with necessary circuit diagram and waveforms. | 6M |
| 6 | a) Write short notes on
(i) Boost regulator (ii) CUK regulators | 6M |
| | b) The dc-dc converter has a resistive load of $R=10\ \text{ohms}$ and the input voltage is $V_s=220\text{V}$. When the converter switch remains on, its voltage drop $V_{ch}=2\text{V}$ and the chopping frequency is $f=1\text{KHz}$. If the duty cycle is 50% determine (i) the average output voltage (ii) the rms output voltage (iii) the converter efficiency (iv) the effective input resistance of the converter. | 6M |
| 7 | a) What is an inverter? With help of circuit and waveforms explain the operation of single phase bridge inverter. | 6M |
| | b) Draw the waveforms and discuss the performance of following methods of PWM control used in inverters. (i) Symmetrical multiple pulse modulation (ii) Sinusoidal pulse width modulation | 6M |
| 8 | a) Explain the three phase thyristorised bridge inverter with star connected resistance load, assuming 120° mode of operation. Draw the corresponding output phase and line voltage of inverter. | 6M |
| | b) A basic three phase bridge inverter is supplied from a 600V source. For a star connected resistive load of $15\Omega/\text{phase}$. Find the RMS load current, the load power and the thyristor ratings for (i) 120° conduction (ii) 180° conduction | 6M |

VARDHAMAN COLLEGE OF ENGINEERING**(AUTONOMOUS)**

Two Year M. Tech I Semester Supplementary Examinations September - 2012

(Regulations: VCE-R11)**POWER ELECTRONIC CONTROL OF DC DRIVES****(Power Electronics and Electric Drives)****Time: 3 hours****Max Marks: 60****Answer any FIVE Questions. All Questions carry equal marks****All parts of the questions must be answered in one place only**

1. a) Explain the continuous and discontinuous modes of operations of a single – phase fully controlled rectifier control of separately excited motor. 6M
 b) A 230 V, 960 rpm, 20A separately excited motor has an armature resistance and inductance of 1.2Ω and 50mH respectively and is controlled by a single – phase half controlled rectifier with source voltage of 230V, 50Hz. Calculate speeds and developed torques on the boundary between continuous and discontinuous conduction for $\alpha = 45^\circ, 90^\circ$ and 135° . 6M
2. a) With a neat circuit diagram, explain the working of three phase full wave controlled bridge converter with separately excited DC motor load for continuous conduction mode. Draw the output voltage and current wave forms for $\alpha = 30^\circ$. 6M
 b) What is the effect of freewheeling diode when it connected across the motor load in three phase full wave controlled bridge converter fed separately excited DC motor. Derive the expression for average load voltage. 6M
3. a) Explain the operation of 3-phase naturally commutated bridge circuit with inductive load as rectifier and inverter. 6M
 b) Discuss the effect of connecting capacitors on the supply side in three phase bridge circuit with passive load impedance. 6M
4. a) Explain the analysis of control modeling of three – phase converter of DC motor drives. 6M
 b) Explain the steady state analysis of two quadrants 3 phase converter controlled DC drive. 6M
5. a) Explain step-by-step derivation of a DC machine transfer function. 6M
 b) Draw the flow chart for the simulation of a single – quadrant phase controlled DC motor drive. 6M
6. a) Explain the steady state analysis of chopper controlled DC motor drive. 6M
 b) A 200-hp, 230V, 500-rpm separately excited DC motor is controlled by a Chopper. The chopper is connected to a bridge – diode rectifier supplied from a 230 V, 3 Phase and 50Hz ac main. The motor chopper details are $R_a = 0.04 \Omega$, $L_a = 0.0015 \text{ H}$, $K_b = 4.172 \text{ V/rad/sec}$, $f_c = 2 \text{ kHz}$. The motor is running at 300 rpm with 55% duty cycle in a chopper. Determine the average current from steady state current waveform and the electromagnetic torque produce in the motor. 6M

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7. a) Explain Hysteresis- current for the closed loop speed controlled separately – excited DC motor drive. 6M
b) Draw and explain the block diagram of PWM current controller implementation with ramp carrier signal for chopper controlled DC motor drives. 6M
8. a) Sketch the flow chart for dynamic simulation of the chopper controlled DC motor drive and explain. 6M
b) Establish the DC motor and speed controller equations in terms of state variables for dynamic simulation of Chopper fed DC motor. 6M

VARDHAMAN COLLEGE OF ENGINEERING**(AUTONOMOUS)**

Two Year M. Tech I Semester Supplementary Examinations September - 2012

(Regulations: VCE-R11)**ADVANCED MICRO PROCESSOR AND MICRO CONTROLLERS****(Power Electronics and Electric Drives)****Time: 3 hours****Max Marks: 60****Answer any FIVE Questions. All Questions carry equal marks****All parts of the questions must be answered in one place only**

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| 1 | a) What is meant by segmentation? Explain how the physical address is calculated from the effective address of data. | 6M |
| | b) With an example, explain different Assembler Directives. | 6M |
| 2 | a) Explain maximum mode operation of 8086 microprocessor with timing diagrams. | 6M |
| | b) Explain Pin diagram of 8086 Micro Processors. | 6M |
| 3 | a) Write an 8086 ALP to relocate a string of length 10 words from 2000H:4000H to 6000H:4000H using string instructions only. | 6M |
| | b) What is type2 interrupt? Explain the condition for initiating type 2 interrupt. | 6M |
| 4 | a) Draw the architectural diagram of 80486 processor and explain in detail about each block. | 8M |
| | b) What is the main difference between the 80386 DX processor and 80386 SX processor. | 4M |
| 5 | a) With a neat sketch explain how DRAM is interfaced. | 6M |
| | b) Describe how A/D and D/A computers can be interfaced | 6M |
| 6 | a) What is the necessity of serial communication interface? Explain command and status register formats in 8251. | 6M |
| | b) Explain various modes of operations of 8253 programmable timer. | 6M |
| 7 | a) Discuss the functioning of timing and control unit and oscillator block of 8051 | 6M |
| | b) Describe the internal RAM organization of 8051 | 6M |
| 8 | a) Develop 8051 ALP to copy 15 bytes of data from External program memory 2000H-200EH to internal data memory 30H-3EH respectively. | 6M |
| | b) Draw and discuss the formats and bit addresses of IE and IP registers and write an instruction sequence to enable all interrupts. | 6M |