QUESTION BANK

Year: III II Branch: CSE Subject: CO Name of the Faculty: V. Surendar

Unit-1

BASIC STRUCTURE OF COMPUTERS : Computer Types, Functional unit, Basic OPERATIONAL concepts, Bus structures, Software, Performance, multiprocessors and multi computers. Data Representation. Fixed Point Representation. Floating – Point Representation. Error Detection codes.

1. Explain about sign magnitude and 2's complement approaches for representing the fixed point numbers. Why 2's complement is preferable.
2. Give means to identify whether or not an overflow has occurred in 2s complement addition or subtraction operations. Take one example for each possible situation and explain. Assume 4 bit registers. (Feb 2008 set 1)
3. Explain about various buses such as internal, external, backplane, I/O, system, address, data, synchronous and asynchronous.
4. Distinguish between error detection and correction codes. What do you understand by odd parity and even parity? What is odd function and even function?. To calculate odd and even parity values which functions can be used? Calculate Odd and even parity values for all hexadecimal digits 0-9 and A-F. (Nov 2007 set 3)
5. Explain about daisy chain based bus arbitration.(Nov 2007 set 4)
6. Convert the following decimal numbers to the bases indicated.
    i. 7562 to octal
    ii. 175 to binary
    iii. 1938 to hexadecimal.(Dec 2009 set 1)
7. Explain types of computers and their areas of applications.
8. Explain the functional unit of a computer system. (Dec 2009 set 2)
9. Make out differences between Multiprocessors and Multi computers.(Dec 2009 set 3)
10. Explain the Bus structure of a computer system with neat bus interconnection scheme diagram. (Dec 2009 set 4)

Unit-2

REGISTER TRANSFER LANGUAGE AND MICROOPERATIONS : Register Transfer language.Register Transfer Bus and memory transfers, Arithmetic Mircrooperatiaons, logic micro operations, shift micro operations, Arithmetic logic shift unit. Instruction codes. Computer Registers Computer instructions
– Instruction cycle.
Memory – Reference Instructions. Input – Output and Interrupt. STACK organization. Instruction formats. Addressing modes. DATA Transfer and manipulation. Program control. Reduced Instruction set computer.

1. What is the use of buffers. Explain about tri-state buffers. Explain about high impedance state.
2. Explain commonly employed bit shift operators such as shift left, right, circular shift left/right and arithmetic shift left/right. Assume an 8-bit register, give an example for each? (Feb 2008 set 2)
3. Design a circuit to increment, decrement, complement and clear a 4 bit register using RS flip-flops. Explain the control logic.(Feb 2008 set 3)
4. Design registers selection circuit to select one of the four 4-bit registers content on to bus. Give fuller explanation.(Nov 2007 set 2)
5.What are register transfer logic languages? Explain few RTL statements for branching with their actual functioning. (Nov 2007 set 4)
6. Explain about instruction, fetch, and decode cycles for a memory reference instruction. Draw a flow chart also to explain the same. Indicate clearly where and which processor registers comes into picture. Now let us assume while a instruction is in the middle of its decode cycle a interrupt is arrived. What is going to happen? Is the instruction is completed or not. If we want to stop there itself and handle the interrupt what are the difficulties?(May 2009 set 3)

7. What is the difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register?
8. Give the 3 instruction code formats of a basic computer.(Dec 2009 set 1)
9. Describe the instruction cycle with the help of a neat diagram. Also draw the flow chart for the same. (Dec 2009 set 2)
10. List the various registers of a computer system. Explain the function of each register.
11. Briefly explain about shift micro operations of computer system.(Dec 2009 set 3)
12. Draw a Bus system for four registers using Multiplexers. Explain it in detail.
13. Explain 4-bit Address Subtracted using a neat diagram.(Dec 2009 set 4)

Unit-3

MICRO PROGRAMMED CONTROL : Control memory, Address sequencing, microprogram example, design of control unit Hard wired control. Microprogrammed control

1. Explain about stack organization used in processors. What do you understand by register stack and memory stack?
2. Explain how X= (A+B)/(A-B) is evaluated in a stack based computer.(Feb 2008 set 1) (Nov 2007 set 3)
3. Write about direct, indirect, register direct, register indirect, immediate, implicit, relative, index, and base address mode of addressing. Why do we need so many addressing modes? Is the instruction size influenced by the number of addressing modes which a processor supports? State whether the number of addressing modes will be more in RISC or CISC? (Nov 2007 set 1)
4. Support the statement Instruction Set Architecture has impact on the processors micro architecture. (Feb 2008 set 4) (Nov 2007 set 4)
5. Why do we need subroutine register in a control unit? Explain. (Nov 2007 set 1)(May 2009 set 4)
6. Why do we need some bits of current microinstruction to generate address of the next microinstruction? Support with a live example. (May 2009 set 3)
7. How do you map micro-operation to a micro instruction address. (Nov 2007 set 3)
8. Describe how microinstructions are arranged in control memory and how they are interpreted.
9.Explain any eight addressing modes in detail.(Dec 2009 set 1) (Dec 2009 set 3)
10.Explain the characteristics of RISC. (Dec 2009 set 3)
11. Convert the expression $A + B * C + (D + E) * F$ into reverse polish notation.
12. Write a program to evaluate the arithmetic statement $X = (A + B) * (C + D)$.
    i. Using a general register computer with two address instructions.
    ii. Using stack organized computer with zero address operation instruction. (Dec 2009 set 2)
13. Explain the two ways of organizing a stack in computer system.
14. Write a brief note on sub routine call and return. (Dec 2009 set 4)

Unit-4

COMPUTER ARITHMETIC : Addition and subtraction, multiplication Algorithms, Division Algorithms, Floating – point Arithmetic operations. Decimal Arithmetic unit Decimal Arithmetic operations.

1. Explain the variety of techniques available for sequencing of microinstructions based on the format of the address information in the microinstruction.
2. Hardwired control unit is faster than micro programmed control unit. Justify this statement. (Feb 2008 set 2)
3. What is overflow and underflow? What is the reason? If the computer is considered as infinite system do we still have these problems? (Feb 2008 set 3).(Feb 2008 set 4) (Nov 2007 set 1) .(May 2009 set 1)
4 .Explain about the micro programmed control organization.
5. Explain the microinstruction format for control memory. (Dec 2009 set 1)
6. Explain address sequencing in micro programmed control unit and also explain mapping of instruction. (Dec 2009 set 2) (Dec 2009 set 4)
7. Describe the design of control unit.((Dec 2009 set 3)
8. Differentiate Micro programmed control and Hardwired control.

Unit-5

THE MEMORY SYSTEM : Basic concepts semiconductor RAM memories. Read-only memories Cache memories performance considerations, Virtual memories secondary storage. Introduction to RAID.

1. "In paged segmentation, the reference time increases and fragmentation decreases", Justify your answer.
2. A Virtual Memory System has an address space of 8K words and a Memory space of 4K words and page and block sizes of 1K words. Determine the number of page faults for the following page replacement algorithms:
   1) FIFO
   2) LRU
3. Explain the following with applications for each:
   (a) ROM
   (b) PROM
   (c) EPROM
   (d) EEPROM.
4. What are the different types of Mapping Techniques used in the usage of Cache Memory? Explain. {Or} Explain the following Cache Mapping Techniques
   (a) Direct Mapping
   (b) Set Associative Mapping. [2007 Nov]
5.. (a) What is a virtual memory technique? Explain different virtual memory techniques. (2007 NOV)
   (b) Explain how the technique of paging can be implemented
   (c) Give the detailed picture of Memory Hierarchy.
6. Explain the following. (Dec 2009)
   (a) Writing into Cache.
   (b) Address space and memory space.
   (c) Performance considerations of Cache memory.
7. Explain about the following: (Dec 2009)
   i. RAM.
   ii. ROM.
8. What do you mean by Address space and Memory space?

Unit-6

INPUT-OUTPUT ORGANIZATION : Peripheral Devices, Input-Output Interface, Asynchronous data transfer Modes of Transfer, Priority Interrupt Direct memory Access, Input –Output Processor (IOP) Serial communication; Introduction to peripheral component, Interconnect (PCI) bus. Introduction to standard serial communication protocols like RS232, USB, IEEE1394.

1. What are the different kinds of I/O Communication techniques? What are the relative advantages and disadvantages? Compare and contrast all techniques.
2. Explain bit oriented and character oriented protocols in serial communication.
3. What are the different issues behind serial communication? Explain.
4. Explain the following:
   (a) Isolated Vs Memory mapped I/O
   (b) I/O Bus Vs Memory Bus
   (c) I/O Interface
   (d) Peripheral Devices.
5. Explain the following:
   (a) Asynchronous Serial Transfer
   (b) Asynchronous Communication Interface.
6. (a) What is Direct Memory Access? Explain the working of DMA.
   (b) What are the different kinds of DMA transfers? Explain.
   (c) What are the advantages of using DMA transfers?
7.(a) What is polling? Explain in detail.
   (b) What is daisy chaining? Explain.
8. Explain the following (2007Nov)
   (a) CPU - I O P Communication
   (b) I O P
   (c) IBM 370 I/O Channel.

9. What is parallel priority interrupt method? Explain with neat sketch.

Unit-7

PIPELINE AND VECTOR PROCESSING : Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, RISC Pipeline Vector Processing, Array Processors.

1. Explain the following with related to the Instruction Pipeline
   (a) Pipeline conflicts
   (b) Data dependency
   (c) Hardware interlocks
   (d) Operand forwarding
   (e) Delayed load
   (f) Pre-fetch target instruction
   (g) Branch target buffer
   (h) Delayed branch.
2. (a) What is pipeline? Explain.
   (b) Explain arithmetic pipeline.
3 Explain pipeline for floating point addition and subtraction.
4 Explain four segment pipelining.
5. Explain three segment instruction pipelines. Show the timing diagram and show the Timing diagram with data conflict.
6. What is pipeline? Explain space-time diagram for Pipeline.
7. Write short notes on the following: [NOV 2007]
   (a) RISC pipeline
   (b) Vector processing
   (c) Array processors.
8. Explain the following in related with Vector Processing (May 2009)
   (a) Super Computers
   (b) Vector operations
   (c) Matrix multiplication
   (d) Memory interleaving.

Unit-8

MULTI PROCESSORS : Characteristics or Multiprocessors, Interconnection Structures, Interprocessor Arbitration. InterProcessor Communication and Synchronization Cache Coherance. Shared Memory Multiprocessors

1. (a) What are the different physical forms available to establish an inter-connection network? Give the summary of those.
2. Explain time-shared common bus Organization.
3. Explain system bus structure for multiprocessors.
4. What is cache coherence and why is it important in shared memory multiprocessor systems? How can the problem be solved with a snoopy cache controller?
5. (a) Explain the working of 8 x 8 Omega Switching network.
   (b) Explain the functioning of Binary Tree network with 2 x 2 Switches. Show a neat sketch.
6. What is the functioning of cross bar switch network? Explain. With a neat sketch. (NOV 2007)
7. How many switch points are there in a cross bar switch network that connect 'p' Processors to 'm' Memory modules.
5. What are the different kinds of Multi stage switching networks? Explain with neat sketch. Compare their functioning. {2007 NOV}, (Dec 2009)
6. What is Multiprocessor? Explain its characteristics. (Dec 2009)

7. Write short notes on multi-port memory. (Dec 2009)
8. (a) Discuss about Flynn's classification of computers.
   (b) Explain about communication topologies used in multiprocessors. (Nov 2007 set 1)