Part A Questions

1. What is stored program concept?
2. Differentiate memory write and I/O write.
3. What are the various methods of accessing data from memory?
4. Define memory cycle time.
5. State the different phases of instruction cycle.
6. What is indirect indexed addressing?
7. What are the fields or flags contained in a PSW?
8. Name few approaches to deal with conditional branching while pipelining.
9. What is a micro operation?
10. What is the use of control memory?
11. List out the basic functions that a computer can perform.
12. List out the performance parameters of memory.
13. _____memory is read and written electrically as with PROM.
14. List out the requirements for an I/O Module.
15. Give the rule for forming the negation of integer in sign-magnitude representation.
16. The collection of different instructions that the CPU can execute is referred to as the CPU's _____.
17. _____ contains the instruction most recently fetched.
18. What is loop buffer?
19. _____ Control unit contains complex logic circuitry for sequencing through the many micro operations of the instruction cycle.
20. Classify micro instructions.
21. _____ and _____ are stored in a single read write memory.
22. External memory capacity is typically expressed in terms of _____.
23. Adjacent tracks are separated by_____.
24. Convenience and efficiency are two objectives of _____.
25. An instruction format defines the layout of the bits of an _____.

26. Define Write data.
27. Expand HLL.
28. Expand RISC.
29. The organization of a multiprocessor system can be classified as _____.
30. Expand PVR.
31. Fetched instruction is loaded into a register in the processor known as ----------.
32. In a ---------- memory, information decays naturally or is lost when electrical power is switched off.
33. List out the drawbacks of programmed and Interrupt-driven I/O.
34. The ---------- converts data from electrical to other forms of energy during output and from other forms to electrical during input.
35. State the rule for finding negation of an integer in Two's Complement notation.
36. List out basic logical operations.
37. List out two categories of CPU registers.
38. What is programmed Exception ?
39. ---------- holds the address of the next instruction to be fetched.
40. List out the two basic tasks that control unit perform.
41. A processor whose elements have been miniaturized into one or a few integrated circuits is called _____.
42. The collection of paths connecting the various modules is called the _____.
43. A more attractive form of read-only memory is _____.
44. Data are transferred to and from the disk in _____.
45. _____ instructions operate on the bits of a word as bits rather than as numbers.
46. The _____ has a 36 bit word length and a 36 bit instruction length.
47. _____ contains the address of a location in memory.
48. _____ contains a variety of status and condition bits.

49. _____ are the functional or atomic operations of a processor.
50. The set of microinstructions is stored in the _____.
51. _____ is a popular high-bandwidth, processor-independent bus that can function as a mezzanine or peripheral bus.
52. _____ is intended to give memory speed approaching that of the fastest memories available, and at the same time provides a large memory size at the price of less expensive types of semiconductor memories.
53. In a _____, there is one read-write head per track.
54. An I/O module that takes on most of the detailed processing burden, presenting a high-level interface to the processor, is usually referred to as an _____.
55. When _____ occurs, the ALU must signal this fact so that no attempt is made to use the result.
56. A _____ is one in which the most significant digit of the significant is zero.
57. _____ contains the address of an instruction to be fetched.
58. Internal memory consisting of a set of storage locations called _____.
59. _____ module interfaces to devices that communicates 1 bit at a time.
60. The _____ contains the address of the next micro instruction to be read.
61. What is a Peripheral?
62. What is an Interrupt Request Signal?
63. Why is associative access fast?
64. State the applications of SRAM and DRAM.
65. State the Overflow Rule.
66. What is an Assembler?
67. State the need for Internal Processor Bus.
68. List the reasons, which complicate the design and use of Pipelines.
69. What is the purpose of MBR?
70. What are Hard Microprograms?

71. _____ register contains the word to be stored in memory, or is used to receive a word from memory.
72. _____ contains the address of next instruction to be fetched from memory.
73. _____ is the volatile memory.
74. In _____ mode the IO module and main memory exchange data without processor involvement.
75. In _____ addressing mode the operand is present as a part of instruction.
76. Write the formula for register addressing mode.
77. _____ contains the instruction most recently fetched.
78. In _____ register of Pentium processor contains condition codes and mode bits.
79. What is the use of MAR?
80. What are the two main task performed by micro programmed control unit?
81. _____ holds the address of the next instruction to fetch.
82. _____ provides storage internal to the CPU.
83. How are bits stored in dynamic RAM?
84. 8086 based systems use one _____ interrupt controller.
85. Which bit is designated as the sign bit in the signed magnitude representation of an integer?
86. What is immediate addressing?
87. Why are general purpose registers present in CPU?
88. What is PSW?
89. Mention the two types of control unit.
90. A sequence of microinstructions is known as micro-program or _____.
91. What is meant by function?
92. Define Interrupt.
93. Define Transfer Rate.

94. List out the drawbacks of programmed interrupt I/O.
95. What is Sign Magnitude Representation?
96. Define instruction set.
97. What general roles are performed by CPU registers?
98. What is a Program Status Word?
99. Define Micro Operations.
100. What is the function of program counter?
101. List out the main structural components of a Computer.
102. What is the expansion for HPC.
103. The two traditional forms of RAM used in computers are _____.
104. What is a Buffer?
105. DOUBLE represents how many numbers of bits in IEEE745 format?
106. Write the basic algorithm for Indirect addressing mode.
107. What is the function of a Stack pointer?
108. Which instruction is used to determine the opcode and the operand specifiers?
109. Give the full form for MAR and MBR.
110. List out the restart instructions available in 8085 microprocessor.
111. State the significance of a Cache memory.
112. List any two exceptional conditions that cause trap interrupts.
113. Classify the storage devices based on speed.
114. Differentiate RAM and ROM.
115. Define assembly level language.
116. Differentiate an operand and an operator with an example.
117. State the definition and role of a register.
118. Name the major phases of a RISC pipeline.
119. Draw the generic format of a control unit.
120. Categorize microinstructions based on their size.
121. What is hardwired program?

122. Number of blocks in main memory is ---------- if number of bits used to address a word is 'n' and the number of words in a fixed block is 'K'?
123. State drawbacks of Interrupt-driven I/O.
124. What is SDRAM? How is it different from DRAM?
125. Compute $(1.0000000010 \times 2^5) - (1.0000000000 \times 2^{-2})$ and normalize the results.
126. State the difference between arithmetic shift and logical shift.
127. State the usage of branch history table in pipelining.
128. A pipelined processor with 5 stages executes a program with 10000 instructions which are issued at a rate of one/clock cycle. What is the speedup factor of this processor compared to non-pipelined processor?
129. Give an example of a horizontal microinstruction.
130. Show the micro-operations for 'Indirect Cycle'

Part B Questions

1. Differentiate computer architecture and organization
2. Differentiate spatial and temporal locality.
3. What are the elements of machine instruction?
4. State the role of the registers involved in instruction execution.
5. What are the rules to group micro operations?
6. Describe the role of cache memory.
7. Compare memory mapped I/O and isolated I/O.
8. List out different elements of a machine instruction.
9. What is Interrupt Vector Table?
10. State the use of Incrementer / Decrementer Address Latch.
11. Draw the functional view of the computer.
12. List out the key characteristics of computer memory system.
13. Define direct addressing mode.
14. Draw the instruction cycle diagram.

15. Draw the control unit micro architecture diagram.
16. Classify different memory accessing methods.
17. What do you mean by cycle stealing?
18. Give the block diagram of Hardware for Addition and Subtraction.
19. List out different flags (or) condition codes in the Program Status Word register.
20. Classify the micro operations.
21. Explain Moore's law.
22. Differentiate SRAM and DRAM.
23. What are the characteristics of twos complement representation of arithmetic?
24. What are the types of flags in PSW? Explain.
25. List the three types of control signals. Explain.
26. What are the key characteristics of computer memory systems?
27. What is ROM? What are the types of ROM?
28 List the types of operands. Explain.
29. What are the general rules performed by the CPU?
30. How is the horizontal micro instruction interpreted?
31. State the design concepts followed in Von Neumann architecture.
32. Compare Memory-Mapped and Isolated I/O.
33. What is a Stack Frame?
34. List out the data flow during an Interrupt Cycle.
35. What are the design considerations of Microinstruction Sequencing technique?
36. Briefly discus three main performance parameter of memory.
37. Explain the concept of processor communication.
38. Explain various forms of integer representation.
39. Draw the internal structure of CPU.
40. Explain various input and output function of control unit.
41. What is an interrupt? When does an interrupt occur?
42. Describe briefly about the programmed I/O.

43. How to represent a binary floating number in IEEE format.
44. Give a neat sketch for the state diagram of the instruction cycle and Explain.
45. Describe about the functions of the control unit with a diagram.
46. Briefly discuss two approaches to deal with multiple interrupts.
47. What are the key properties of semiconductor memory?
48. List out the elements of a machine instruction.
49. Write short notes on interrupts and exceptions.
50. What basic tasks does a control unit perform?
51. What is an Interrupt?
52. What is meant by Access time?
53. List out the elements of Machine instruction.
54. Draw and explain the concept of the Instruction cycle.
55. Write a short note on LSI-11 microinstruction sequence.
56. Name and brief any five major components of computer organization.
57. List the steps involved in Interrupt driven I/O with a suitable pseudo code from the view of an I/O module.
58. Explain the types of instruction with suitable example.
59. State about condition code register.
60. Write a short note on Intel 8085 control unit.
61. Write about the performance parameters of memory.
62. Consider a machine with byte addressable main memory of 2^{32} bytes and block size of 16 bytes. Assume a set associative cache consisting of 4K lines divided into two-line sets. How is the address divided into tag, set and byte number?
63. Perform two's complement integer multiplication for (-7) x (3)
64. Write a short note on interrupt vector table in Pentium processor
65. Write short notes on Wilkes control

Part C Questions

Question Bank

1. Explain instruction cycle in detail with state diagram.
2. Explain the bus structure and its architecture.
3. What is the need for a mapping function in cache memory? Explain the various mapping Techniques used in cache?
4. Explain various RAID levels.
5. a.Explain the various instruction types.
   b.Explain the action taken by CPU for various types of operations.
6. Explain the various addressing techniques with their relative advantages and disadvantages.
7. a.Explain instruction cycle.
   b.Illustrate the effect of a conditional branch on instruction pipeline operation.
8. Explain instruction pipeline and evaluate its performance and speedup.
9. What are the functional requirements of a control unit? Elaborate on control signals and data paths in a control unit.
10. Explain micro instruction sequencing.
11. Describe about Cache design. Explain different mapping functions in detail.
12. Explain different components of computer system with neat block diagram of its top level view.
13. Describe about Interrupt driven I/O. Explain design issues is implementing Interrupt driven I/O.
14. Explain about Advanced DRAM Organization.
15. Explain Booth algorithm for Two's Complement Multiplication.
16. Enumerate different types of operations and explain them in detail.
17. Explain the Register Organization of the CPU.
18. Explain Intel 80486 Pipelining mechanism in detail.
19. Explain the Hardware Implementation of Control Unit.
20. Describe about Micro Instruction Sequencing in detail.
21. Draw the architecture of a Computer and explain its functions.

22. What is the need for Cache memory? Explain the Cache memory management in detail.
23. With neat block diagram explain DMA.
24. Explain programmed I/O in detail.
25. Explain various types of operands with suitable example.
26. Briefly explain various addressing modes.
27. Discuss in detail about Instruction Pipelining and explain it.
28. Briefly explain on Instruction Cycle.
29. Explain Hardwired implementation in detail.
30. Explain the micro operations in the control unit of a computer.
31. State the need for Page Replacement algorithm in cache memory. Explain different Page Replacement Strategies in detail.
32. Explain how does multiple Interrupt handling carry out.
33. Describe about semiconductor main memory organization. Explain different semiconductor main memories in detail.
34. Explain Direct Memory Access (DMA) in detail.
35. Explain unsigned Binary Multiplication with neat block diagram. Analyze the multiplication processing by giving sample input data for multiplicand and multiplier.
36. Describe about Pentium Operation Types in detail.
37. Analyze the Register Organization of Pentium Processor.
38. Explain different approaches for dealing with pipelined execution of conditional branch instruction execution.
39. Explain the functional requirements for the control unit to control the CPU.
40. Explain micro programmed control unit and its functioning in detail.
41. Explain about the bus inter connection in detail.
42. Discuss about the elements of cache memory design.
43. Discuss about the semiconductor main memory.
44. a.Discuss about the programmed I/O.
    b.Explain about the interrupt driven I/O

45. Explain the multiplication of unsigned and two's complement number with example.
46. Discuss about the machine instruction characteristics.
47. Explain about the instruction cycle in detail.
48. Discuss about the Pentium processor architecture in detail.
49. Discuss about the control of processor.
50. Explain about the micro operation sequencing.
51. Discuss about the structure and function of the computer.
52. Explain about the interrupts with instruction cycle.
53. Discuss about the Magnetic Disc in detail.
54. a.Explain about the direct memory access with suitable diagram.
    b.Explain about the I/O channels and processors.
55. Explain the floating point arithmetic with flow chart in detail.
56. Discuss the different types of addressing modes.
57. Explain about the register organization in a general computer.
58. Discuss about the instruction pipeline in detail.
59. How does the concept of micro operations serve as a guide to the design of control unit? Explain in detail.
60. Write short notes on:
    a.Micro operations
    b.Micro programmed control unit
61. Describe the approaches used to deal with multiple interrupts.
62. Explain Cache organization and Cache Read operation.
63. Describe the use of Hamming Code in error correction.
64. Explain the functions and structure of an I/O Module.
65. Explain hardware implementation of unsigned binary multiplication.
66. Describe the Pentium Addressing Modes.
67. Discuss Register Organization in the Processor.
68. Describe the branch prediction techniques.
69. Explain the functional requirements for the control of the Processor.
70. Explain the functioning of Microprogrammed Control Unit.

71. Discuss the various elements of cache design.
72. Discuss with neat diagram the top level view of computer components.
73. Discuss various functions of I/O modules.
74. Discuss Interrupt driven I/O in detail.
75. Discuss the block diagram and hardware implementation of unsigned binary multiplication with suitable example.
76. a.Draw and explain block diagram of addition and subtraction unit.
    b.Briefly explain the steps of Booth multiplication for twos complement number.
77. Discuss CPU instruction cycle in detail.
78. Briefly discuss the CPU instruction pipelining.
79. Discuss various sub classes of instruction cycle.
80. Discuss the functioning of micro programmed control unit with neat sketch.
81. With a diagram, explain the structure and functions of the CPU and control unit.
82. Give the typical organization of cache, design considerations and its operation.
83. a.Draw the structure of Dynamic RAM and mention its features.
    b.Explain static RAM and its operations.
84. a.How does the CPU determine which device issued the interrupt in an Interrupt driven I/O? Explain.
    b.Explain in detail about DMA.
85. a.Explain Booth's algorithm with a flow chart and example.
    b.Give the flowchart for unsigned binary division.
86. a.Explain about the transfer of control in an assembly language program with an example.
    b.Explain about the Pentium addressing modes.
87. Explain the concept of instruction pipelining and dealing with branches.
88. a.Write about the interrupt processing in Pentium processors.
    b.Describe about the Intel 80486 pipelining.

89. Draw the organization of the Intel 8085 key components and explain.
90. What are the two ways of implementing the control unit? Explain Wilke's control micro programmed control unit and write about the taxonomy of microinstructions.
91. Explain in detail about the top-level view of the computer components.
92. Discuss in detail about the Cache Memory.
93. With a neat diagram, explain in detail about the Synchronous Dynamic RAM (SDRAM).
94. Explain in detail about the Direct Memory Access.
95. Discuss in detail about the different types of Operations.
96. Explain in detail about the different types of Addressing Modes.
97. Explain about the Instruction Cycle with its state diagram.
98. Discuss in detail about the Intel 80486 Pipelining with example.
99. Explain in detail about the functions of Micro Programmed Control.
100. Discuss in detail about the Microinstruction Sequencing.
101. Explain in detail about the Functions of a Computer.
102. Briefly explain the concept of the elements of Cache design.
103. With a neat sketch explain in detail about the advanced DRAM organization.
104. Give in detail about various Error correcting methodologies.
105. Briefly explain the concept of Transfer control instructions.
106. Explain in detail about Pentium and Power PC addressing modes.
107. With a neat sketch explain the organization of the Power PC processor.
108. Explain the concept of Instruction Pipelining.
109. Draw and explain the architecture of 8085 microprocessor.
200. Explain the instruction execution methods for Microinstructions.
201. Classify and brief different types of interrupts and corresponding applications in details.
202. With suitable examples, illustrate various addressing modes employed.
203. Explain various types of ROMs and RAMs that are used in today's applications.

204. With neat diagrammatic narration, explain the operating mechanism of DMA controller.
205. With a suitable example, narrate various Flynn's operands and operations.
206. Explain the Pentium and PowerPC addressing modes in details.
207. List out and explain various registers and their functionality.
208. Explain the six stages of pipelining process and how it ensures parallelism.
209. What is a firmware? Explain how the firmware control unit is implemented.
210. Illustrate microinstruction sequencing and execution in detail.
211. Discuss with neat diagram the top level view of computer components and detail about the basic instruction cycle.
212. Explain in detail about cache read operation and direct mapping function.
213. How will you detect and correct single bit error in 8-bit words using Hamming error-correcting code. Explain using a 8-bit error data.
214. What is programmed I/O? Explain the role of the processor in programmed I/O using relevant block diagrams.
215 Draw and explain block diagram of unsigned binary division and perform the calculation for '(0110)/(0010)'.
216. Explain in detail about the most common transfer-of control operations found in instruction sets.
217. a.Briefly discuss about instruction pipelining with 6 pipeline stages (FI, DI, CO, FO, EI, WO). If the 5th instruction is a 'conditional branch' instruction and jump to 20th instruction in memory, explain the effect of conditional branch instruction using timing diagram.

    b.State the different approaches to deal with conditional branches in pipelining processors
218. Explain in detail about register organization in a general computer.
219. Explain the Hardware Implementation of Control Unit with an example.
220. Describe about micro instruction sequencing in detail. What are the address generating techniques?